HUMAN MACHINE INTERFACE/BRAIN CONTROL FOR ELECTRIC VEHICLES APPLICATION

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<td>Human Machine Interface</td>
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<tr>
<td>EV</td>
<td>Electrical Vehicle</td>
</tr>
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<td>BCI</td>
<td>Brain Computer Interface</td>
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<td>EEG</td>
<td>Electroencephalogram</td>
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<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
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<tr>
<td>AFE</td>
<td>Analog Front-End</td>
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<td>ADC</td>
<td>Analog-to-Digital Converter</td>
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<td>CMFB</td>
<td>Common Mode Feedback</td>
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<td>CMFF</td>
<td>Common Mode Feedforward</td>
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<td>DRL</td>
<td>Driven Right Leg</td>
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<td>TDM</td>
<td>Time Division Multiplexing</td>
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<td>CS</td>
<td>Chopping Stabilization</td>
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<td>Noise Efficiency Factor</td>
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<td>PEF</td>
<td>Power Efficiency Factor</td>
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<tr>
<td>ETI</td>
<td>Electrode-Tissue-Impedance</td>
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<td>SVM</td>
<td>Support-Vector Machine</td>
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<td>Abbreviation</td>
<td>Full Form</td>
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<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
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<tr>
<td>IA</td>
<td>Instrumentation Amplifier</td>
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<tr>
<td>PGA</td>
<td>Programmable Gain Amplifier</td>
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Abstract

Human machine interface (HMI) that provides easy-to-use and effective interaction between human and Electric Vehicles (EV) has attracted remarkable research interests. Various HMI approaches have been reported to improve the driving experience and enhance safety. Among different potential candidates, Electroencephalogram (EEG) is a promising approach by recording brain signals with the electrodes on the scalp and decoding the signaling with real-time brain signal processing. Since body movement is not required to generate the signaling, risks of distraction to the driver is minimized.

Multi-channel analog front-end (AFE) is a key building block in HMI for EV applications. This work describes the design of four AFE for wearable HMI in EV applications. Firstly, a 4-channel TDM-based EEG AFE is presented which focuses on the improvement of Common Mode Rejection Ratio (CMRR). A system-level innovation of combining chopping stabilization (CS) and time division multiplexing (TDM) is proposed to achieve a system-level CMRR enhancement. Secondly, the same design methodology is extended to a 16-channel TDM/CS AFE with tunable DC-servo loop and fine-trimming input impedance boosting loop. A 4-bit calibrated impedance boosting loop contributed to the input impedance of 560 MΩ as well as CMRR for input interface. A tunable DC-servo loop (TDSL) is designed to cancel the maximum input DC offset of 200 mV at a controlled speed so that the TDSL achieves a fast cancellation for the input DC offset without any glitch injection. Thirdly, a novel area-efficient driven-right leg (DRL) circuit is proposed for multi-channel neural recording AFE. A capacitor-free DRL structure is proposed which
provides a 60-dB enhancement of system-level CMRR, with 90% area reduction for the DRL circuit. Finally, a low-power, low-noise bio-potential recording AFE is developed with enhanced power efficiency factor (PEF) performance. The AFE has obtained the smallest PEF under ultra-low power supply of 0.5 V with power consumption of 2 µW and a low input-referred noise of 2.1 µVrms that is achieved by high-frequency chopping scheme.
Chapter 1

Introduction

1.1 Background

The Human Machine Interface (HMI) that serves as a tool for communication between human and machine, has enabled users to take charge of fuzzy machines with ease. Within recent decades, a large area of application for HMI has been explored in the market. With the increasing number of interacting modalities, HMI has been developed for use in some new applications such as nuclear power plant [1], laparoscope [2], driver assistance [3]-[5] and robots [6]. In order to control mechanical devices, HMI collects signals from users as command and reflects the status of the operating process. A conventional HMI which contains a bulky control table, real buttons and numerous wires, cannot meet the requirement for ambulatory interaction. Therefore, a growing trend of wireless and wearable HMI has been reported [7]-[9].

The Electric Vehicles (EV) deploys electricity as its power is one of the most eco-friendly mobiles. With advancements in recent years, EV has become more and more popular. The development of HMI in EV is shown in Figure 1.1, illustrating the replacement of the ancient symbols by interactive display and virtual messages at the front window. Moreover, automotive display sizes are growing from 2.0-inch (2.x) to more than 10.0-inches (10.x+), which provides sufficient area for notification
of necessary information and user-interaction. A good HMI design can certainly improve on the performance, usability, and security for EV.

![Figure 1.1 Development of HMI in Electric Vehicles (EV) [10]](image)

Considering safety and flexibility for drivers in EV, a user-friendly HMI should provide sufficient information for interaction as well as avoiding distraction on the road. Moreover, as safety requirement becomes more stringent, an advanced HMI is not just a tool to transmit information to the driver, but a monitor for data collection to detect the driver’s vigilance status since much evidence has indicated that drivers’ drowsiness has become the key factor in many road accidents [11] - [15].

Drowsiness detection has been studied and implemented by various methods in recent years. Some research focused on the physical changes while fatigue driving [16] - [20]. A number of movement such as eye blinking, relaxing posture and the decreased gripping force on the steering wheel can be used as inclination signals for drowsiness detection. Since these movement signals are directly detected by the
sensors in the chair and steering wheel or captured by cameras as shown in Figure 1.2, these techniques provide a non-contact way for real-time vigilance status monitoring, which is widely accepted by drivers. However, the target parameters, such as the frequency of posture changing and force on the wheel differs a lot from person to person. Moreover, the various types and conditions of electrical vehicles and environments have increased the risk of false report.

Figure 1.2 A typical eye-tracking drowsiness detection system [21]

Another kind of drowsiness detection in HMI is to use biological signals such as eye blinking, heart rate, body potential and Electroencephalography (EEG) signal to monitor the vigilance status of drivers [22] – [37], which is shown in Figure 1.3. Biological signal, which is released from intrinsic body, can replace traditional movement signals such as body posture and finger pressing.
Nowadays, EEG signal is considered as one of the potential information carrier for drowsiness monitoring in the future. Moreover, an EEG-based HMI sets user’s hands free and helps people with physical disabilities to complete tasks such as braking and navigation.

By placing multiple sensing electrodes on the user’s scalp, the voltage fluctuation between any two nodes is recorded as EEG signal. The EEG signal records electrical potentials produced by primary current within the apical dendrites of the pyramidal neurons of the cerebral cortex [39]. EEG signal can be used to distinguish epileptic seizure from other neurological disorder in clinical area. Moreover, the EEG patterns recorded simultaneously by multiple channels can be classified and transformed as specific commands by the support-vector machine (SVM) [40].
1.2 Motivation and Challenges

The EEG-based HMI provides a great opportunity for drivers in EV to communicate with vehicles without body movement. As shown in Figure 1.4, a helmet with electrodes on driver’s head can translate individual brain activities to real instructions. EEG signal fluctuation can be recorded and observed by the EEG-based HMI, to trigger the emergency braking system in EV to prevent any potential traffic accidents [41].

![Figure 1.4 A simulated EEG-based HMI for braking system in vehicles [41]](image)

Due to some limitations of the EEG signal, an EEG-based HMI raises several challenges:

1) **Electrode offset**: gel-based wet electrodes is the first choice during clinical therapy for its low impedance, while considering the ease of use in ambulatory environment, dry electrodes should be chosen for wearable HMI applications. However, dry electrodes suffer from high electrode-tissue
impedance (ETI), which causes performance degradation and should be suppressed.

2) **Common mode interference**: EEG signal, due to its small amplitude (1 μV~100 μV), can be easily ruined by its correlated large common mode interference. An analog front-end interface for EEG acquisition with high common mode rejection ratio (CMRR) is essential in EEG-based HMI.

3) **Person-to-person variation**: the amplitude of EEG signal varies significantly among people, hence leading to difficulty for pattern recognition and machine learning. A large database is required for classification and real-time analysis. Therefore, hardware integration, as well as area consideration becomes an important issue.

4) **Noise disturbance**: in consideration that the EEG signals (α, β, θ and δ waves) are mainly located around the baseband (from 0.5 Hz to 100 Hz), which suffers from the detriment of flicker noise, a low noise analog front-end interface is necessary for ensuring good EEG signal quality.

According to the challenges of EEG-based HMI, a low noise, high CMRR analog front-end interface must be carefully designed for EEG acquisition. Moreover, the electrode mismatch shall be considered for system-level CMRR calculation.
1.3 Objectives

A multi-channel EEG recording system is to be developed to facilitate research on EEG-based HMI for EV applications. Multiple EEG signals from the sensing electrodes will be recorded simultaneously, and sent for classification in a digital processing unit.

In this project, multiple dry electrodes will be connected to the input of each channel, and the common reference recording montage will ensure that the voltage difference between the sensing node and reference node on the scalp is processed in an independent channel. Therefore, this chip contains multiple channels for amplifying EEG signal from dry electrodes, and the outputs will be digitalized in ADC and classified in SVM.

The objective of this project is to design an analog front-end interface for EEG-based HMI in EV. The primary goals for this design include the followings:

- To improve the system-level CMRR for the analog front-end recording circuit of the EEG acquisition system. The CMRR of the entire recording system should be more than 100 dB to avoid large common mode interference.
- To develop a low power architecture for the analog front-end interface. With the increasing number of recording channels, power consumption for each recording channel should be within μW range for long term monitoring.
- To suppress noise within the frequency range of EEG signal. A low noise analog front-end interface will be proposed to obtain the EEG signal from a
noisy environment. Several techniques for noise reduction should be applied to this front-end circuit.

1.4 Organization

The structure of this thesis is organized as follows:

Chapter 1 provides the background information on human machine interface (HMI), EEG based HMI and the motivations for the EEG recording system.

Chapter 2 presents literature review of the previous works on EEG recording IC. The general design considerations for EEG recording interface are included and a comparison of various CMRR enhancement techniques is also given.

Chapter 3 introduces a 4-channel TDM based analog front-end prototype for EEG-based HMI. A system-level CMRR enhancement scheme is proposed in this chapter, and detailed circuit explanation for noise reduction and power saving techniques are included.

Chapter 4 presents a 16-channel TDM based AFE for wearable EEG applications. The proposed design is an extended version of the design in Chapter 3, which includes a TDM/Chopping capacitive-coupled instrumentation amplifier with a fine-trimming input boosting loop and a tunable DC servo loop.

In Chapter 5, a 10-channel AFE for neural recording system is proposed with an area-efficient driven right leg (DRL) circuit for system level CMRR improvement. Instead of using the TDM/CS technique proposed in Chapter 3 and 4, the novel DRL
circuit in this chapter improves system-level CMRR as well, and has saved 90% chip area when compared to traditional DRL circuit.

Chapter 6 proposes a low power, low noise bio-potential amplifier under 65nm CMOS technology. Besides CMRR enhancement, power/noise performance should be considered as well. The proposed design has a wide bandwidth for various bio-signal recording under an ultra-low voltage supply. An optimal balance among power, noise and bandwidth has been achieved by this design.

Chapter 7 summarizes the current research progress and draws the conclusion. Some future works for the analog front-end interface of wearable EEG-based HMI are briefly discussed which includes the chopping ripple reduction and offset cancellation techniques.
Chapter 2

Literature Review

2.1 EEG-Based HMI for Electrical Vehicles applications

Electroencephalogram (EEG) recording is a noninvasive method for real-time analysis of brain function [42]. A tester’s scalp, which works as the source of EEG signal, provides different kinds of inputs for the acquisition system such as slow waves, evoked potentials (EPs), event-related de-synchronization/event-related synchronization (ERD/ERS) and delta-theta activities [43] - [47].

As mentioned in Chapter 1, EEG-based HMI collects EEG signal from driver’s brain and sends it to the dedicated processor for interaction in EV. The function of EEG-based HMI for EV applications are drowsiness detection [38], indoor localization [48], and emotion prediction [49]. With the help from EEG-based HMI, drivers’ safety and mental status can be monitored without any intentional operation when driving on the way.

2.1.1. Type of EEG Signal

There are four types of normal EEG waves: alpha (8-12 Hz), beta (14-30 Hz), theta (4-7 Hz) and delta (<3.5 Hz). The four types of EEG signal are shown in Figure 2.1. The signal power of these waves decreases exponentially as frequency increases [42]. Conventionally, the amplitude of EEG signal is within ±40-60 μV. These EEG waves reflect different kinds of brain activities, emotion and health state.
Alpha wave occurs in a frequency range from 8 to 12 Hz. This rhythmic wave can be found when a person is awake in a resting state. Alpha wave is produced most intensively in the occipital region while it can still be recorded from the parietal and the frontal region of the scalp. The Amplitude of alpha wave is about 20 µV to 200 µV and this kind of EEG signal can be detected while closing eyes.

Beta wave is located at higher frequency from 14 Hz to 30 Hz and can be as high as 50 Hz during intense mental activity. There are two kinds of beta wave, beta I and beta II in both parietal and the frontal region. Beta I wave is affected in a similar way with alpha wave while beta II appears with strong activation of central nervous system, which means these two kinds of beta waves restrict each other during mental activities.

Theta wave has a lower frequency of 4-7 Hz. This kind of EEG wave has higher possibility of appearing in children while it can also be found in some adults when they are stressful and repress to an action. Some experiments verify the occurrence of theta wave by offering a person some pleasant experience at first, then suddenly
taking away the amusing elements from this tester. A period of 20 seconds of theta wave can be found at the same time.

Delta wave is defined as all the rest of EEG waves which are located below 3.5 Hz. This EEG wave occurs frontally in adults while posteriorly in children. Delta wave has the largest amplitude among the four types of EEG signals. And this wave can be used to verify some serious organic brain diseases.

2.1.2. Electrode Selection

Based on the characteristic of EEG waves, the electrodes which are used for picking up these biological signals should be carefully selected. In order to maintain high quality of EEG signal, the impedance of electrodes should be made small enough to avoid noise detriment. However, the electrodes are not always directly connected to the tissue on the scalp, and leave some space between electrode and tissue, which makes the electrode-tissue-impedance (ETI) too large to conduct the small voltage fluctuation of EEG signal. Therefore, the electrode gel is usually applied to connect the electrode and skin seamlessly.

Figure 2.2 Typical equivalent models of recording electrodes [51]
As shown in Figure 2.2, there are three typical electrodes: wet electrode, dry contact electrode and dry non-contact electrode. For the electrode tissue interface, there are some coupling layers between the electrode and surface of scalp, which can be described as parallel RC elements [51].

![Figure 2.3 Dry electrodes and caps for wearable EEG acquisition system [52]](image)

Figure 2.3 Dry electrodes and caps for wearable EEG acquisition system [52]

Wet electrode is a good choice for EEG recording in clinical applications. By injecting electrolyte gel on the electrodes, the model of ETI becomes a two-layer-combination of RC elements. With the help of conductive gel, the ETI of wet electrodes can be as low as a few KΩ. But the hair on scalp should be abraded or hydrated to achieve low impedance during EEG recording, and be washed for gel removal after the experiments. Wet electrodes are suitable for clinical use and has an optimal signal accuracy of EEG monitoring. However, the inconvenient procedure predicts that this kind of electrodes cannot be used in ambulatory applications.

Dry contact electrodes are developed for wearable EEG recording devices as shown in Figure 2.3 Several gold-coated pins are built on the sensing plate to form a direct contact with skin. The length of the pin is adjustable so that the dry electrodes can reach the surface of scalp appropriately. By wearing a special cap with labeled
standard positions for electrode placement, as shown in Figure 2.3, dry electrodes can be attached to the scalp without the need for conductive gel. Considering user convenience, dry electrodes should be chosen for wearable EEG-based HMI applications. The drawback of using the dry electrode is the large electrode-tissue impedance of the dry contact electrode varies from several hundreds of KΩ to a few MΩ, which has been studied and optimized to approach the similar performance as wet electrodes [53]. Moreover, the dry contact electrodes are fixed and attached to the user’s scalp by wearing a special EEG cap to avoid cable movement. However, the pressure on the scalp from the pins of the dry contact electrodes makes it uncomfortable for users.

Dry non-contact electrodes provide a more user-friendly interacting solution for wearable EEG applications. The non-contact electrode can be integrated to various garments and the EEG signal will be capacitive coupled from the human scalp to the electrodes. However, the non-contact electrodes have a higher electrode-tissue impedance than the contact electrodes. The electrode area, cloths hair and air gap between the scalp and the electrodes have an important impact on the electrode impedance.

2.1.3. Recording Montage

One of the critical limitations of EEG recording is the spatial resolution, but it can be improved by increasing the number of electrodes. The 10-20 system is an international standard for EEG recording placement on scalp. As depicted in Figure 2.4, different nodes are labeled with letters and numbers. The letters F, T, C, P and
O stand for frontal, temporal, central, parietal area and occipital lobes, respectively while the numbers represent the locations on each specific area. For example, the even numbers stand for the nodes on the right hemisphere and zero refers to the midline of the scalp. With the help of this international standard, an individual’s research achievement can be discussed and compared with each other.

![Diagram of EEG electrode placement]

Figure 2.4 The 10-20 system for EEG recording electrode placement [54]

The EEG source reconstruction accuracy depends on numerous factors, including the specific inverse approach, the accuracy of the head model volume-conductor and the EEG electrodes montage [55]. There are three normal types of EEG recording montage, and they are described as follows:

- **Bipolar montage**: Each channel (waveform) represents the difference between two adjacent electrodes. The entire montage consists of a series of these channels. For example, the channel “Fp1-F3” represents the difference in voltage between the Fp1 electrode and the F3 electrode. The next channel in the montage, “F3-C3,” represents the voltage difference between F3 and C3, and so on through the entire array of electrodes.
• **Common Reference montage:** Each channel represents the difference between a certain electrode and a designated reference electrode. There is no standard position for this reference; it is, however, at a different position than the “recording” electrodes. Midline positions are often used because they do not amplify the signal in one hemisphere vs. the other. Another popular reference is “linked ears,” which is a physical or mathematical average of electrodes attached to either earlobes or mastoids.

• **Average reference montage:** The average reference montage consists of a series of derivations in which all of the electrodes are added together in input 2 of every amplifier to serve as a reference for each electrode. However, one electrode or more electrodes can dominate the final value of the reference. Because the average reference usually contains all the scalp electrodes, the electrode in input 1 is compared against the other electrode.

### 2.2 ExG-based HMI for Electrical Vehicles Application

The development of CMOS technology has stimulated the progress of biomedical devices towards low power, low noise, highly integrated system with fuzzy functionalities [100 - 102]. The sensing interface, which converts the biomedical signal into voltage fluctuation via AFEs, is a critical block in biomedical recording systems. For various biomedical signals, such as EEG, ECG and EMG signals, there is a growing trend to integrate the different recording AFEs into one recording block to save hardware resource as well as power consumptions [103-105].

Moreover, for EV applications, an ExG (EEG, ECG and EMG) -based HMI is able to monitor driver’s mental status, heart rate as well as muscle abnormalities. While there is not much work integrate the ExG with neural signals. The amplitude
and frequency of the EEG, ECG, EMG, Local Field Potential (LFP) and Action Potential (AP), as shown in Figure 2.5, varies and overlaps each other.

![Figure 2.5 Comparison of the amplitude and frequency of ExG, neural LFP and AP](image)

### 2.3 System Overview

The EEG recording system consists of several parts, and Figure 2.6 shows a typical system. The EEG signal is picked up by dry/wet electrodes attached on user’s scalp and sent to operational amplifier. The amplified analog signal is converted to digital output by analog-to-digital converter (ADC), and then transmitted to the digital back-end unit for feature extraction and classification. The final output will be sent to the device controller as specific command of HMI.

![Figure 2.6 A typical EEG recording system](image)
Considering the performance of dry electrodes, the active electrode is a preferred choice especially for wearable EEG recording system. This is because the integration of the dry electrode and the preamplifier can minimize noise pick-up, and the low output impedance can suppress the cable motion artifacts [56]. The use of preamplifier also helps to relax noise requirement of the following amplification stages.

Table 2.1 Comparison of commercial dry EEG recording system

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor type</td>
<td>Dry</td>
<td>Dry and active</td>
<td>Dry</td>
<td>Dry</td>
<td>Dry</td>
<td>Dry and active</td>
</tr>
<tr>
<td>Bandwidth (Hz)</td>
<td>0.23 – 125</td>
<td>0 – 50</td>
<td>0 – 50</td>
<td>3 – 100</td>
<td>0.02 – 120</td>
<td>0.5 – 100</td>
</tr>
<tr>
<td>Resolution (Bits)</td>
<td>24</td>
<td>24</td>
<td>24</td>
<td>12</td>
<td>16</td>
<td>12</td>
</tr>
<tr>
<td>No. of channels</td>
<td>4</td>
<td>16/24/32/64</td>
<td>8/20</td>
<td>1</td>
<td>23</td>
<td>8</td>
</tr>
<tr>
<td>Sampling rate (Hz)</td>
<td>128/256/512</td>
<td>300</td>
<td>500</td>
<td>512</td>
<td>240/960</td>
<td>1024</td>
</tr>
<tr>
<td>Transfer</td>
<td>wireless</td>
<td>Wireless</td>
<td>wireless</td>
<td>wireless</td>
<td>wireless</td>
<td>Wireless</td>
</tr>
<tr>
<td>Weight (g)</td>
<td>100</td>
<td>350</td>
<td>65</td>
<td>90</td>
<td>500</td>
<td>NA</td>
</tr>
<tr>
<td>Battery life (Hour)</td>
<td>23</td>
<td>6</td>
<td>16</td>
<td>8</td>
<td>24</td>
<td>22-70</td>
</tr>
</tbody>
</table>
Some commercial dry EEG recording system has been listed in Table 2.1. Most of them are suitable for hairy surface of the users. A wireless transfer is preferred for data transmission and the weight of the most products is less than 500 g, which is affordable for wearing on the head. Although some results [60] – [61] show that the accuracy of the dry EEG system is not sufficient compared with wet EEG system, the other work present promising results for signal quality.

Ambulatory EEG recording can be used in clinical for epilepsy detection [68], and a four-channel EEG acquisition system has been used in a Brain Computer Interface (BCI) application [69]. The low-density system is not usually welcome by clinical use. In fact, a typical commercial EEG system with 256 channels is mostly preferred. Another system with 600 channels is proposed to avoid spatial aliasing [70]. However, in case of battery life and system complexity, the channel count in a wearable EEG device should be selected without accuracy degradation.

Since the EEG-based HMI requires a large database for signal analysis, multi-channel recording is a basic requirement for EEG acquisition system. The most commonly used architecture is the common reference montage which will compare every node to a reference node. This structure saves hardware cost as well as chip area, at the cost of CMRR degradation, which will be discussed in the following chapter.

A detailed study on multi-channel EEG acquisition system for ambulatory application is conducted by Refet Firat Yazicioglu [71]. As shown in Figure 2.7, an 8-channel ASIC design is used for common reference montage recording. The fine
and coarse low pass filters (LPF) are placed on the feedback path of the core instrumentation amplifier (IA) to remove electrode offset. A chopper-stabilized IA is used for noise reduction, while the entire gain can be adjustable with variable gain amplifier (VGA). Impedance measurement and calibration mode are implemented in this ASIC design, the former technique is used for user to monitor electrode impedance while the latter one enables gain calibration for each recording channel. Although the CMRR of each IA can be as high as 120 dB, the system-level CMRR is not discussed in this paper.

Figure 2.7 An 8-channel EEG acquisition ASIC [71]

Another design proposed by Jerald Yoo [72] realizing the integration of front-end acquisition interface and classification processor is shown in Figure 2.8. This scalable SoC is divided into an eight-channel analog front-end interface, a 10-bit
fully differential SAR ADC, a patient-specific machine-learning seizure classification processor, a SRAM and external interfaces [72]. The gain and bandwidth of the analog front-end can be configured by the digitally-assisted analog signal processing unit (ASPU). There are eight Feature Extraction Engines, a Classification Engine and a channel controller inside the classification processor. With the scalable recording channels, which is decided by the system clock, this SoC can support three recording montages: bipolar, common reference and averaged reference montage. A machine-learning algorithm is implemented for the patient-specific seizure detection. However, CMRR of this system is not presented in this paper yet.

Figure 2.8 An 8-channel scalable EEG acquisition SoC [72]
The recent reported EEG acquisition system by Jiawei Xu [73] is designed for wearable EEG system with dry electrodes. As shown in Figure 2.9, traditional electrodes are integrated with preamplifier as active electrode (AE). The common mode feedforward (CMFF) technique improves the system-level CMRR by 25 dB, and the PWM modulation enables a single-wire data communication link between AE and BE [73].

![Figure 2.9 A wearable 8-channel active-electrode EEG/ETI acquisition system [73]](image)

### 2.5 Analog Front-end Interface Design Specifications

As the first module of EEG recording, a multi-channel EEG front-end interface should be designed to meet several requirements:
1) **Low noise**: In consideration of the fact that EEG signals (α, β, θ and δ waves) are mainly located around the baseband (from 0.5 Hz to 100 Hz), which suffer from the detriment of flicker noise, a low noise analog front-end interface is necessary for ensuring good signal quality. The flicker noise in baseband should be separated from EEG signal, and then filtered out by LPF.

2) **Low power**: With the increasing number of recording channels, power consumption is considered as one of the most significant parameters for EEG recording. In order to support long term monitoring, an EEG recording system needs to be able to function properly at 1 V supply or even lower.

3) **High CMRR**: EEG signal, due to its small amplitude (1 μV~100 μV), can be easily ruined by large common-mode interference. Because of different recording montage, the definition of CMRR varies, in order to approach high CMRR, several techniques should be considered to boost the system-level CMRR, since the impedance of dry electrode is large comparing with wet electrode, input impedance should be taken into consideration of system-level CMRR.

4) **Optimal PSRR**: for wearable EEG recording devices, the fluctuation of power supply will cause serious problem, especially when the power is supplied by energy harvesting block. Therefore, PSRR is another important specification. Some design techniques should be considered to improve the PSRR to suppress the effect of power fluctuation. Battery is usually the preferable choice for power supply for such wearable recording system.
For the clinical EEG applications, there are two medical standards as shown in Table 2.2, which draws up requirements for electrical performance of analog front end (AFE) in terms of noise, bandwidth, DC offset tolerance, CMRR, etc. The standard IEC 60601 stands for the safety and effectiveness of medical electrical equipment, published by the International Electrotechnical Commission. And the standard IFCN is the standards of International Federation of Clinical Neurophysiology.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>IEC 60601 [74]</th>
<th>IFCN [75]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application</td>
<td>Clinical EEG</td>
<td>Clinical EEG</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>0.5 mVpp</td>
<td>NA</td>
</tr>
<tr>
<td>Input referred noise</td>
<td>6 µVpp</td>
<td>0.5 µVrms (0.5 – 100 Hz)</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>0.5 – 50 Hz</td>
<td>0.17 – 70 Hz</td>
</tr>
<tr>
<td>DC offset tolerance</td>
<td>300 mV</td>
<td>NA</td>
</tr>
<tr>
<td>Input Impedance @50/60Hz</td>
<td>NA</td>
<td>&gt; 100 MΩ</td>
</tr>
<tr>
<td>CMRR@50/60Hz</td>
<td>NA</td>
<td>100 dB</td>
</tr>
<tr>
<td>Safe DC current</td>
<td>50 µA</td>
<td>NA</td>
</tr>
</tbody>
</table>

The most important parameters for EEG analog front-end interface are reported above in Table 2.2. However, the two standards are for clinical use of biomedical equipment. In order to meet the requirement of a low-power, low noise analog front-end interface with high system-level CMRR for wearable EEG recording system, design specifications are summarized in Table 2.3 based on the two international
standards. Dry electrode is usually selected for wearable EEG applications, due to its large electrode-skin impedance, the AFE should be designed with stringent parameters such as higher input impedance and CMRR to ensure an optimal signal quality.

Table 2.3 Design specifications for wearable EEG analog front-end interface

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1 V</td>
<td></td>
</tr>
<tr>
<td>No. of Channels</td>
<td>&gt;4</td>
<td></td>
</tr>
<tr>
<td>Intrinsic CMRR for amplifier</td>
<td>&gt;120 dB</td>
<td>Enough headroom for CMRRPD</td>
</tr>
<tr>
<td>System-level CMRR</td>
<td>&gt;80 dB</td>
<td></td>
</tr>
<tr>
<td>Input Referred Noise</td>
<td>&lt;0.8 $\mu$V rms (0.5 – 100 Hz)</td>
<td>As low as possible</td>
</tr>
<tr>
<td>Average power/channel</td>
<td>&lt;2 $\mu$W</td>
<td>Low power</td>
</tr>
<tr>
<td>Gain</td>
<td>1000</td>
<td>60 dB</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>0.5 – 100 Hz</td>
<td></td>
</tr>
</tbody>
</table>

2.6 CMRR Analysis

Since the amplitude of typical EEG signal is about 10 $\mu$V to 100 $\mu$V, which is easily ruined by the common mode interference (up to 200 mV). The common mode rejection ratio (CMRR) becomes a key parameter to evaluate the performance of EEG acquisition system.

CMRR is defined as the rejection ratio of unwanted common signal of both input leads to the wanted differential signal. An ideal differential amplifier will have infinite CMRR, which is not practical in real case of amplifier design.
As reflected in equation (1), the output of an ideal amplifier only depends on the differential gain and input differential signals. The practical output of the amplifier is really the sum of amplified differential signal and common signal.

\[ V_o = A_d (V_+ - V_-) + \frac{1}{2} A_{cm} (V_+ + V_-) \quad (1) \]

where \( A_d \) is the differential mode gain of the amplifier while \( A_{cm} \) is the common mode gain.

The definition of CMRR for single amplifier is shown in equation (2), which is the ratio of the differential gain to common mode gain. In order to restrict common mode interference to the noise level, the intrinsic CMRR of the recording amplifier should be more than 100 dB.

\[ CMRR = 20 \log \left( \frac{A_d}{A_{cm}} \right) \quad (2) \]

Figure 2.11 bio-potential recording system in common reference montage
While the common-reference montage is used in a bio-potential recording system as shown in Figure 2.11, the bio-signal $V_{out}$ is defined as the difference of two channels’ output. The between-channel CMRR, i.e. $CMRR_{chn}$ is defined as equations (3) - (7); where $\Delta G_A$ is the gain mismatch of two input pair and $G_A$ is the averaged gain of the amplifier [76].

\[
V_{out} = G_{A1} V_{in1} - G_{A2} V_{in2} \tag{3}
\]

\[
V_{out} = \frac{G_{A1} + G_{A2}}{2} (V_{in1} - V_{in2}) + \left( G_{A1} - G_{A2} \right) \frac{V_{in1} + V_{in2}}{2} \tag{4}
\]

where the differential input and common input are derived in Equation (5):

\[
V_{DM} = V_{in1} - V_{in2} \tag{5}
\]

\[
V_{CM} = \frac{V_{in1} + V_{in2}}{2} \tag{6}
\]

Therefore, the CMRR for the input pair is derived in (8):

\[
CMRR_{chn} = \frac{G_{DM}}{G_{CM}} = 20 \log \left( \frac{G_{A1} + G_{A2}}{2(G_{A1} - G_{A2})} \right) = 20 \log \left( \frac{G_A}{\sqrt{V_A}} \right) \tag{7}
\]

Therefore, for the case of a common reference montage used in a two-channel recording system, the between-channel CMRR depends on the gain mismatch of the two channels, some technique such as automated gain adaption [77] has been implemented to improve the $CMRR_{chn}$. 

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2.7 CMRR Enhancement Techniques

Some useful techniques have been proposed for CMRR enhancement for amplifiers, while there are several methods to improve system-level CMRR. The most common methods are common mode feedback (CMFB), common mode feedforward (CMFF) and driven-right-leg (DRL). The specific structure and principle of each technique is described as follows.

1) Common Mode Feedback

![Figure 2.12 CMFB technique in single-ended amplifier](image)

When using single-ended amplifier as the first amplification stage, CMFB is usually the most effective approach for cancelling the common mode voltage. In Figure 2.12, the output of A1 is filtered by a low pass filter to attain the common mode voltage. The resulting common mode voltage is then sent to the input of the amplifier A2, and the output of A2 is feedback to the non-inverting input of amplifier A1. Hence, the new CMRR with CMFB is derived:
\[
CMRR = CMRRg20\log \left( \frac{2A_v}{2 + \frac{1}{A_{v,CMFB}}} + 1 \right) \tag{8}
\]

\[
CMRR' = CMRRg20\log \left( A_v \right) \tag{9}
\]

\(A_v\) is the close loop gain of \(A_1\) and \(A_{v,CMFB}\) is the gain of \(A_2\). CMFB is also effective for multi-channel recording system; as in [78], the averaged common mode voltage is feed to the non-inverting input of each pre-amplifier. This method reduces the effective common mode voltage and enhances the CMRR of each input pair by \(20\log (A_v)\) where \(A_v\) is the gain of each pre-amplifier.

Unfortunately, CMFB requires a summing amplifier which consumes extra power and requires a low-pass filter with high precision for dc voltage filtering. Moreover, a large capacitor is needed for miller compensation of stability. All of these add-ons will consume extra power and area.

2) Common Mode Feedforward

![Common Mode Feedforward Diagram](image)

Figure 2.13 CMFF technique in single-ended amplifier
Considering the drawbacks of CMFB technique, another design using the common mode feed forward (CMFF) is proposed as shown in Figure 2.13. In this scheme, a settled-up common-mode voltage is directly fed to the input of amplifier. And a resistor and capacitor is used to decide the value of common-mode voltage. While compared with the CMFB technique, the biggest difference is the common mode voltage, which is directly sent to the input instead of passing through a stage amplification in the feedback loop. This improves the stability of the entire system with no extra power and area consumptions. According to Equation (8), the improved CMRR for CMFF is derived as follow:

\[
CMRR = CMRR + 20 \log \left(1 + \frac{R}{sC} \right)
\]  

(10)

However, this method still has some drawbacks, the common mode voltage of various recording nodes change by time while a pre-defined common mode voltage cannot be calibrated. This method is thus not suitable for long term monitoring. Also, the additional resistor and capacitor bring in more thermal noise during the first stage of amplification, hence ruining the quality of the input signal.

3) Driven Right Leg Circuit

Comparing with the technique of CMFF and CMFB techniques, the driven right leg (DRL) is an ancient method proposed in 1983 to reduce the common mode voltage. This method is similar to the CMFB technique except for the common mode
voltage is fed back to human body through another electrode in DRL circuit. This helps to reduce the filtering process.

![Driven Right Leg circuit for CMRR enhancement](image)

As Figure 2.14 shows, $C_s$ is the stray capacitance between the amplifier common and earth ground and $C_b$ is the stray capacitance between the body and earth ground. The CMRR improvement is derived as equation (11) – (14):

\[
V_c = -GV_o, G = \frac{2R_f}{R_d} 
\]

\[
V_c = V_o - R_{e3}i_d 
\]

\[
V_c = R_{e3}i_d, R_c = \frac{R_{e3}}{G+1} (13)
\]

\[
\therefore CMRR = 20\log(G_{DRL})gCMRR
\]  

If the third electrode is connected directly to common, the effective resistance between the patient and common is the electrode resistance $R_{e3}$ [79]. Equation (14)
shows that if the third electrode is connected to a driven right leg circuit, then the
effective resistance $R_c$ and common mode voltage $V_{cm}$ are reduced by the feedback
loop gain. Therefore, the system-level CMRR is improved by the gain of DRL loop.

However, this method suffers from stability issue, whereby the feedback path
introduces an RC pole to the original circuit. The gain of the DRL circuit cannot be
made too large; otherwise the system cannot guarantee a phase margin of 45 degree.
Typically, the gain of DRL circuit can provide 30 dB at the power line frequency,
which is very limited for CMRR enhancement.

In the previous design, DRL circuit is usually constructed by off-chip
components, which put the coupling components and amplifier on the PCB, while
some recent designs proposed recording blocks with on-chip DRL circuit. Although
the design techniques are the same, compared with off-chip DRL circuit, the
mismatch of the passive components can be improved if DRL circuit is implemented
on-chip. However, for multi-channel recording system, the passive components
consume large die area for the on-chip DRL block.

2.8 Summary

In this chapter, the characteristics of EEG signal, recording electrodes and
recording montages have been introduced, then some existing EEG recording
systems are reviewed. Focus on the CMRR characterization, the CMRR analysis are
proposed in this chapter and finally some CMRR enhancement techniques including
common mode feedback, common mode feedforward and driven-right leg circuit are
presented.
Chapter 3

Design A: TDM-Based 4-Channel Analog Front-end

3.1 Introduction

Electroencephalogram (EEG) is an electrophysiological method to record the electrical activities of brain. EEG is an essential tool in applications such as epileptic seizure detection, sleep disorder monitoring and non-invasive human-machine interface. The acquisition of EEG signal is usually through the electrodes placed on the scalp, which provide a mixture of different types of EEG signals such as slow waves, evoked potentials (EPs) and delta-theta activities [80-81].

For EEG-based HMI in EV applications, the major challenge is the small signal amplitude (1 μV to 100 μV). Hence, the EEG signal can be easily ruined by noise and the large common-mode interferences coupled from the vehicle environment, artifacts or other external interferers. Noise and Common Mode Rejection Ratio (CMRR) are thus the two critical parameters for the EEG recording AFE in EV application. To reduce noise, especially for flicker noise, a chopping-stabilized amplifier is a preferable choice for EEG recording analog front-end. To improve CMRR, a few circuit-level techniques such as common-mode feedback (CMFB) [78], common-mode feed-forward (CMFF) [82], driven right leg (DRL) [79] and digital-assisted DRL [83] have been explored for the cancellation of the common-
mode signals. However, all these techniques require extra feedback loop or external biasing block, which may degrade the noise performance or causing stability issue.

Figure 3.1 Block diagram of the proposed TDM/chopping EEG AFE

The block diagram of the proposed multi-channel AFE for wearable dry electrode EEG recording is shown in Figure 3.1. The proposed design adopts a two-stage front-end amplifier for a balance between power and gain. A novel time-division-multiplexing (TDM)/chopping architecture is implemented in the Stage-I of AFE. The output of Stage-I IA is sent into MUX unit and multiplexed to the input of Stage-II IA for further amplification, then the output of the stage-II is demodulated and de-multiplexed to all the channels. In order to avoid flicker noise in both Stage-I and II IA, the input signal is up-modulated through Stage-I and II, and recovered back to its original frequency range in the output of Stage-II. The benefit of this arrangement includes (1) power reduction due to the sharing of 2nd stage amplifier by all channels, (2) system CMRR enhancement (3) chopping stabilization to remove
amplifier low frequency flicker noise. The IA in both stage-I and II operates under supply voltage of 1V while the chop/mux unit works under 1.8 V.

### 3.2 CMRR Analysis

Several CMRR enhancement techniques have been introduced in the previous section. However, those techniques mainly focus on the improvement of the intrinsic CMRR of amplifiers. From a system-level perspective, the definition of system-level total CMRR ($CMRR_T$) depends on both electrode CMRR ($CMRR_E$) and AFE intrinsic CMRR ($CMRR_I$) as shown in Figure 3.2.

![Figure 3.2 Definition of system CMRR for the AFE interface](image)

$CMRR_T$ is represented as:

$$CMRR_T^{-1} = CMRR_E^{-1} + CMRR_I^{-1}$$  \hspace{1cm} (15)$$

where $CMRR_I$ is the intrinsic CMRR of the amplifier and the $CMRR_E$ is caused by the potential divider effect.

For the case of a single channel recording AFE, the electrode CMRR ($CMRR_E$) is derived as:
\[ CMRR_E = \frac{Z_{in}}{Z_e} \]  

(16)

where \( Z_{in} \) is the input impedance of the AFE while \( Z_e \) is the impedance of electrode-skin interface.

For a multi-channel recording system, reference input is connected to all the channels, which degrades both the \( CMRR_E \) and \( CMRR_T \), the \( CMRR_E \) for multi-channel system is derived as [84]:

\[ CMRR_E = \frac{1 + 2 \left( \left| \frac{Z_{in}}{Z_e} \right| \right) + N\alpha}{2(N\alpha - 1)} \]  

(17)

where \( Z_{in} \) is the input impedance of the amplifier and \( Z_e \) is the electrode-skin impedance, while \( N \) is the number of channels which shared the same reference electrode and \( \alpha \) is the mismatch coefficient for the impedance of reference electrode and working electrode. The derivation of Equation (17) is given in Appendix.

### 3.3 Time Division Multiplexing and Chopping Stabilization

The intrinsic CMRR of a fully differential amplifier usually can be as high as 90 dB [84]. However, according to Equation (15-17), \( CMRR_T \) is dominated by \( CMRR_E \) since \( CMRR_E \) is usually smaller than \( CMRR_I \). Considering the case of \( N = 2 \) and \( \alpha = 1 \) (perfect match between reference and working electrodes), \( CMRR_E \) shall be 60 dB under the condition of \( Z_{in}/Z_e = 1000 \). Hence, \( CMRR_T \) normally will be less than 60 dB for the case of two channels sharing the same reference electrode. In
order to improve $CMRR_T$, the number of channels that share the same reference electrode should be reduced to one.

![Signal flow diagram](image.png)

**Figure 3.3** Signal flow of the TDM/chopper stabilization system

One effective method is to use bipolar montage for multi-channel EEG recording system. However, this montage cannot provide a common baseline for the local EEG signal hence is not widely used. For a common reference montage, another effective method is to use the TDM technique to ensure the reference signal is only occupied by single channel within a certain period in time domain. Moreover, only the TDM scheme cannot up-modulate the original EEG signal, which will leave
the EEG signal be ruined by the flicker noise from the amplifier. While chopper stabilization is a well-known technique to overcome flicker noise in biomedical applications, an innovative arrangement is proposed to combine the TDM and chopping stabilization in our design.

The signal flow for the proposed TDM/Chopper stabilization scheme is described in Figure 3.3. The reference signal is firstly sent to one channel with the acquired EEG signal from a working electrode, then the two input signals of this channel are chopped to the chopping frequency before amplification. After stage-I amplifier, a TDM scheme sent the output signals of stage-I from four channels to the shared stage-II one by one. After the amplification in stage II, the chopped and multiplexed signal stream is chopped back to its original frequency, and de-multiplexed to four channels. With the help of chopping stabilization in frequency domain, flicker noise has been reduced in the target frequency range (0.5-100 Hz) while reference signal has been avoided sharing by multiple channels in time domain by TDM technique. Moreover, the amplifier in stage-II is shared by four channels. Thus, the total power consumption and area, are very much reduced for this wearable EEG recording system. $m(t)$ is the transfer function of chopping signal and $s(t)$ is the multiplexing signal as shown in Equation (18-19).

$$m(t) = \sum_{m=0}^{+\infty} \left( \mu \left[ t - mT + \frac{1}{2} \right] - \mu \left[ t - mT - \frac{1}{2} \right] \right)$$

$$s(t) = \sum_{m=0}^{+\infty} \Pi \left( \frac{t - mT - n\lambda}{\lambda} + \frac{1}{2} \right)$$
Figure 3.4 The control strategy for MUX/chopping switches

For circuit-level implementation, two pairs of switches shall be used for multiplexing and chopping as demonstrated in Figure 3.4. In order to avoid charge injection and clock feed-through from the switches, the control circuit is designed with only one pair of switches to facilitate both chopping and multiplexing operations. As shown in Figure 3.5, using just one clock signal and one MUX signal, four control signals can be created for the entire chopping/MUX unit.

Figure 3.5 Digital unit for generation of control signal
3.4 Impedance boosting loop (IBL) with cap-bank calibration

An impedance boosting loop that draws current from the input of the amplifier can help to increase the input impedance as well as contribute to the improvement of $CMRR_E$. As shown in Figure 3.6, the IBL utilizes a 4-bit capacitor bank (25 fF, 50 fF, 100 fF and 200 fF) with a default capacitor of 340 fF to improve the precision of the positive feedback capacitor. The value of the C-bank can vary from 340 fF to 715 fF with minimum step of 25 fF, to compensate for the capacitor mismatch due to chip fabrication.

The recording amplifier adopt a capacitive coupled fully-differential instrumentation amplifier architecture as shown in Figure 3.7 [85], the value of input capacitor $C_{IN}$ is 5 pF while the value of feedback capacitor $C_{FB}$ is 500 fF to obtain the gain of 20 dB. Two back-to-back transistors (1 µm/4 µm) form the pseudo-resistor to provide DC bias for input terminals. The frequency of chopping and time division multiplexing is 2 kHz and 8 kHz for our proposed design, respectively.

![Figure 3.6 Schematic of the amplifier in stage-I with chop/mux and IBL](image-url)
The schematic of the fully differential amplifier for stage I is shown in Figure 3.7. A current-reuse technique is proposed by a pair of input transistor with large size of W/L (200 µm/2 µm and 200 µm/3 µm). With this pair of input transistors operating in subthreshold region, a high gm efficiency is obtained to suppress the input-referred noise within the low frequency range from 0.5 Hz to 100 Hz to be less than 1µVrms, and two pseudo-resistors is used for common mode feedback in the second stage of the amplifier. The current consumption for the core amplifier is only 1 µA with a supply voltage of 1 V.

![Figure 3.7 Schematic of the core amplifier](image)

The IA used in Stage-II is a fully-differential capacitive-coupled amplifier while its core amplifier is the same in Stage-I as shown in Figure 3.7. The gain of Stage-II is 40 dB. The value of input/feedback capacitor is 20 pF/200 fF, respectively. The MUX unit is shown in Figure 3.8, which consists of four transmission gates with
four different control signals. The control signal $V_{T1}$ ($V_{TB}$), $V_{T2}$ ($V_{TB}$), $V_{T3}$ ($V_{TB}$) and $V_{T4}$ ($V_{TB}$) will be selectively turned-on for 25% duty cycle for one MUX period.

![Figure 3.8 Schematic of a) mux unit and b) de-mux unit](image)

### 3.5 Measurement Results

A 4-channel EEG recording AFE test chip has been designed and fabricated in a standard commercial 0.18-µm 1P6M CMOS process. The chip photo of the proposed AFE is shown in Figure 3.9. The area of the overall active circuits and each channel is only 0.3 mm$^2$ and 0.077 mm$^2$ respectively. The current consumption for each channel is only 1.25 µA under 1V supply voltage.

![Figure 3.9 Chip photo of the proposed design](image)
The measured differential mode gain for the proposed design is 60 dB as shown in Figure 3.10. The low cut-off and high cut-off frequency are 0.47 Hz and 1.7 KHz, respectively, which is suitable for EEG signal recording.

![Figure 3.10 AC response for the EEG AFE](image)

The input impedance of the proposed design can be calibrated with different combinations from the 4-bit capacitor, as shown in Figure 3.11. The measured boosted input impedance is 545 MΩ at 50 Hz with a IBL capacitor setting of 0100 and its equivalent value of the IBL capacitor is 440 fF.

With the measured input impedance of the proposed AFE, and supposing the perfect matching for input impedance of the amplifier, the variance of $CMRR_E$ can be calculated according to Equation (4) with the coefficients of electrode impedance ($Z_E$), electrode mismatch ($\alpha$) and the number of channels ($N$) that shared the same reference electrode. Since for the proposed TDM/MUX architecture, there is only one channel operating without sharing the reference with other channels, $N$ equals 1.
for our topology. Then the variance of $CMRR_E$ is depicted in Figure 3.12, for the
difference of electrode impedance from 100 KΩ to 1 MΩ and electrode mismatch
from 1% to 5%, the $CMRR_E$ varies from 80 dB to 115 dB.

Figure 3.11 Input impedance for the EEG AFE with different C-bank settings

Figure 3.12 $CMRR_E$ for different electrode impedance and mismatch at 50 Hz
The input-referred noise density of the proposed EEG interface is given in Figure 3.13. The black line indicates the noise density when the chopper is turned-on. For this case, the input-referred noise is only 40 nV/sqrt(Hz) and 0.72 µVrms, integrated from 0.5 Hz to 100 Hz. While the red line represents the noise density when the chop/mux is turned on, the integrated noise is slightly higher to be 0.76 µVrms from 0.5 Hz to 100 Hz. The blue line represents the noise measured without chop/mux and pink line represents the simulation result when chop/mux turns on. It is clear that the flicker noise is much reduced by using the chopping or chop/mux. Comparing with the simulation result, the current noise is introduced by the charge injection/clock feedthrough from the chopper units in the low frequency range.

Figure 3.13 Input-referred noise for the proposed AFE with different conditions
The measured intrinsic CMRR of the proposed design is presented in Figure 3.14, the $CMRR_I$ is 89 dB at 50 Hz. For a typical case of electrode-skin impedance is 500 KΩ and $\alpha = 1.05$ for 5 % mismatch, the $CMRR_E$ is 82 dB and the total CMRR, i.e. $CMRR_T$ is 81.8 dB.

![Intrinsic CMRR for the proposed AFE](image)

Figure 3.14 Intrinsc CMRR for the proposed AFE

The in-between channel crosstalk is measured as shown in Figure 3.15. Two sinusoid input signals (40 Hz and 100 Hz) with same magnitude are sent to channel 1 and 3, respectively. The measured output magnitude of channel 1 and the leakage signal from channel 3 are -8.1 dBV and -82.6 dBV, respectively. Hence the in-between channel crosstalk is only -74.5 dBV.

The fabricated chip has been tested in human trial for EEG eyes-open / eyes-closing experiments. The spectrum results are shown in Figure 3.16 with two conditions of eye-closing and eye-opening, respective. The red line is the spectrum
of eyes-closing and blue line is for eye-opening. When eyes are closing, there is an obvious periodic α wave comparing with the condition of eye-opening. The peak curve around 8 Hz of the red line indicates the appearance of α wave when eyes are closing.

Figure 3.15 Measured Crosstalk for two channels of the proposed AFE

The performance comparison table among the state-of-the-art designs are shown in Table 3.1. By implementing the TDM/MUX architecture, our proposed 4-channel analog front-end interface circuit achieved the lowest power consumption per channel of only 1.25 µW comparing with the other state-of-the-art designs, while the integrated noise is 0.72 µVrms from 0.5Hz to 100 Hz, which is also better than others. The input impedance of the core amplifier in stage I is boosted by the calibrated IBL to 545 MΩ at 50 Hz, then the $CMRR_e$ is derived as Equation (4) to
be 82 dB with electrode-skin impedance of 500 kΩ and a electrode impedance mismatch of 5%. The $CMRR_I$ measured from core amplifier is 89 dB. Hence the system-level CMRR, i.e. $CMRR_T$ is calculated by Equation (5) to be 81.8 dB, which is the highest $CMRR_T$ among the other designs. The crosstalk is -74.5 dBV for in-between channel crosstalk. And the area per channel is only 0.077 mm$^2$, which is the smallest comparing with others and indicates an area-efficient solution for EEG recording system. In conclusion, our proposed analog front-end interface has fulfilled the various demands for EEG recording system and is suitable for wearable EEG interfacing applications.

Figure 3.16 Measured EEG signal for eyes-open and eyes-closing
### Table 3.1. Comparison Table with The State-of-the-art Works

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<th>[78]</th>
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<td>Wearable EEG</td>
<td>Clinical EEG</td>
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</tbody>
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*CMRR<sub>T</sub> is calculated based on Equation (1) – (3) with electrode-skin impedance of 500 KΩ and α=1.05 for 5% mismatch for dry electrodes, β=1 for perfect matching for the input impedance of the amplifier.

### 3.6 Summary

In this chapter, a 4-channel EEG analog front-end interface for EEG-based HMI in EV applications is designed and fabricated in 0.18 µm CMOS technology. The proposed design deployed an innovative combination of chopping stabilization and time division complexing to achieve a balanced recording structure and high CMRR from the system-level standard. Moreover, the combination of chopping stabilization and TDM techniques provided an optimum and robust solution for the tradeoff between power consumption and noise reduction. A 4-bit calibrated impedance boosting loop contributed to the input impedance as well as CMRR for input
interface. Hence the fabricated analogue front-end achieved a system-level CMRR of more than 80 dB with a typical value of electrode impedance and electrode mismatch. This chop/mux analog front-end obtain an optimal noise performance of 0.72 µVrms integrated from 0.5 Hz to 100 Hz while the power consumption for the entire system is 5 µW and the power per channel is only 1.25 µW. Therefore, the proposed 4-channel analogue front-end is suitable for wearable EEG-based HMI for EV applications.
Chapter 4

Design B: 16-Channel TDM/Chopping Analog Front-end for Wearable EEG Application

4.1 Introduction

Due to the inherent small signal amplitude, EEG signal acquisition usually requires sophisticated electrode setup procedure and high precision signal recording equipment which has bulky size [81]. Therefore, the current EEG monitoring practice is mostly limited to hospital environment.

For EEG-based HMI in EV application, wearable EEG recording is an emerging solution that allows continuous EEG monitoring during driving on the road. Dry electrode is preferred in wearable EEG system because it is easier to setup without skin preparation and usage of conductive gel. However, dry electrode also brings a few design challenges to the recording circuit development. First of all, dry electrode has much higher skin/electrode impedance compared to conventional wet electrode. Therefore, the input impedance of readout circuit needs to be boosted to match with the dry electrode [83]. Furthermore, EEG signal is susceptible to the common-mode interferences coupled from the AC power line, artifacts generated by body movement or other external interference sources. Hence, high common mode rejection ratio (CMRR) is required for the recording circuit. A few CMRR enhancement techniques have been introduced in the literatures. Most of them focus on the improvement of the intrinsic CMRR of amplifier [89]. However, the system
level CMRR is more critical for overall system performance especially for the multichannel acquisition system [84].

A novel TDM based 4-channel analog front-end has been proposed in Chapter III to improve the system-level CMRR while the number of channels in design A is still too small for a typical 10-to-20 EEG recording system.

In this chapter, a 16-channel AFE for dry electrode EEG recording is presented. Time Division Multiplexing (TDM) is combined with chopping stabilization (CS) to improve the system-level CMRR and the AFE input-referred noise. Techniques such as tunable impedance boosting loop, DC-servo loop has been included to boost the AFE input impedance as well as to cancel the input DC offset. The overall performance of the AFE has been optimized for wearable multi-channel EEG recording.

4.2 System Architecture and Circuit Block

The proposed 16-channel EEG system architecture is shown in Figure 4.1. It comprises two identical AFE cells and each has 8 fully differential EEG recording channels. Comparing with design A, this 16-channel design placed the demodulation unit at the output of stage-I instead of stage-II, which releases the bandwidth requirement of the IA in stage-II. Therefore, the flicker noise in stage-II should be suppressed by adjusting the gain distribution in the two stages. In each channel, a two-stage amplifier structure is adopted with 30 dB fixed gain in the 1st stage and a 25/30 dB programmable gain amplifier (PGA) for the 2nd stage. One common reference electrode is shared by all the working electrodes within the cell. A
TDM/CS capacitive coupled instrumentation amplifier (CCIA) is proposed to enhance the system CMRR and noise performance. By controlling the switches in the TDM/CS block, the reference electrode is only connected to one channel during the corresponding signal acquisition time slot. TDM also allows the sharing of 2nd stage PGA among all the channels in the cell by connecting the output of the 1st stages CCIA to the 2nd stage PGA sequentially through a MUX synchronized with the TDM/CS control signal. After demodulation and low pass filter, the output signal go back to the respective channel through a de-MUX. The proposed structure is highly scalable by changing the number of channels in the unit AFE cell.

Figure 4.1 Block diagram of the proposed 16-channel TDM/CS EEG AFE
4.3 TDM/CS Technique

Although CMRR_I of a well-designed fully differential amplifier can be higher than 90 dB [89], CMRR_T is eventually limited by CMRR_E for multichannel AFE. Considering the case of N=2 and α=1 (no impedance mismatch between reference and working electrodes), CMRR_E shall be 60dB under the condition of Z_{IN}/Z_E=1000. The electrode/skin impedance is even higher for dry electrodes (Hundreds of KΩ to MΩ), leading to even lower system CMRR_T. Hence, ideally, the number of channels that share the reference electrode should be reduced to one.

Figure 4.2 (a) The proposed TDM/CS unit, (b) digital unit for control signal generation and (c) timing scheme for TDM/CS switches in 16 channels

The TDM/CS switches schematic is shown in Figure 4.2 (a). The number of the switches have been minimized to avoid the excessive charge injection and clock
feed-through from the switches. As shown in Figure 4.2 (b), The \( \text{CLK}_\text{IN} \) and \( \text{MUX}_\text{IN} \) can generate all the sequential MUX signals (MUX1 to MUX8). The \( \text{CLK}_\text{IN} \) and each sequential MUX signal can generate the four local control signals for the TDM/CS unit. Therefore, only two control signals (\( \text{CLK}_\text{IN} \) and \( \text{MUX}_\text{IN} \)) are required in the digital control unit to generate all the control signals. The timing scheme of the control signals are shown in Figure 4.2 (c), the sequential MUX signals are 1/8 duty cycle clock signals.

### 4.4 CS-CCIA Circuit

The schematic of the proposed CS-CCIA is shown in Figure 4.3 (a). CS technique is adopted to reduce the low frequency flicker noise. To compensate the input impedance drop due to chopping, a positive feedback path for input impedance boosting is implemented with 4-bit fine trimming impedance boosting loop (FIBL). By implementing the FIBL, the current from FIBL equals to the current sent into the input capacitor. Therefore, the current seen from the input node will be much reduced. However, the mismatch of the C-bank and \( C_{FB} \) will causes some current difference between the feedback current through \( C_{FB} \) and FIBL, which degrades the input impedance. The FIBL provides 16 values of the feedback capacitance to avoid the capacitor mismatch due to chip fabrication. The bank consists of a default capacitor of 340 fF and 4-bit trimming capacitor (25 fF, 50 fF, 100 fF and 200 fF), which is manually controlled during testing to see how much the input impedance can be acquired. On the other hand, the input offset voltage can be up-modulated by chopping. Therefore, a tunable DC-servo loop (TDSL) is designed to cancel the input
DC offset. The response time of the TDSL is determined by the time constant of the coupling capacitor $C_{\text{INT}}$ and the tunable pseudo-resistor (TPR). The impedance of the TPR is controlled by the gate voltage $V_G$. During the reset, $V_G$ is controlled in such a way that it is ramped up from GND to VDD at a controlled speed so that the TDSL achieves a fast cancellation for the input DC offset without any glitch injection.

The amplifier core is a fully differential inverter-based OTA shown in Figure 4.3 (b), which is reusing the same structure in design A. The current-reuse technique is employed at the input stage to achieve the required noise performance with minimum current consumption. The two input transistor pairs (PM1-2, NM1-2) are biased in weak inversion region to maximize the current efficiency. Transistors NM3, NM4 provide common-mode feedback and fix the output DC level of the first stage. In the second stage, PMOS transistors are chosen as the input pair to reduce the noise.

Figure 4.3 (a) Schematic of the TDM/CS-CCIA, (b) Schematic of the OTA
4.5 Measurement Results

The proposed AFE chip has been designed and fabricated in a standard commercial 0.18-μm 1P6M CMOS process. The chip photo is shown in Figure 4.4. The chip area of the overall active circuits and each channel is 3.6 mm² and 0.23 mm² respectively. The current consumption for each channel is 1.5 µA under 1V supply voltage. The chopping clock is selected as 4 kHz and the TDM clock frequency is 250 Hz with 1/8 duty cycle. Therefore, the data acquisition window for each channel is sufficient to meet the Nyquist Theorem requirement for information bandwidth up to 100 Hz. The measured voltage gain of two gain settings are 60/54 dB as shown in Figure 4.5. The low cut-off/high cut-off frequency are 0.37/750 Hz and 0.33/950 Hz for the two modes respectively. The measured intrinsic CMRR of the proposed design is presented in Figure 4.6, the $CMRR_I$ is 89 dB at 50 Hz. Assuming 500 KΩ electrode-skin impedance and 5% impedance mismatch ($\alpha = 1.05$) between two dry electrodes, the $CMRR_E$ is 87 dB. With conventional setup, the calculated $CMRR_T$ can be calculated to be 40 dB whereas the $CMRR_T$ with TDM/CS technique is 82 dB, which is enhanced by about 40 dB. The measured input-referred noise density is shown in Figure 4.7. The black line indicates the noise density when the chopper is ON and TDM is OFF. This is equivalent to the setting for single channel chopped amplifier.

The measured input-referred noise floor is only 50 nV/sqrt(Hz) at 100 Hz and the integrated input referred noise is 0.57 µVrms across 0.5 Hz to 100 Hz band. The red line represents the setting when both chopping and TDM signals are ON, the integrated noise is slightly increased to 0.63 µVrms in the same frequency band. This
indicates negligible impact of the TDM scheme to the overall circuit noise performance. The blue line represents the simulation result when chop/mux is on, comparing with simulation results, the measured noise has demonstrated current noise introduced by the chop/mux switches. And the pink line is the result when chop/mux are off, it is clear that the chop/mux has reduced much noise in the low frequency bandwidth (0.5 – 100 Hz).

Figure 4.4 Die photo of the proposed AFE
Figure 4.5 Measured gains of the proposed AFE

Figure 4.6 Measured CMRR_I and calculated CMRR_E and CMRR_T based on Equation (15) – (17) with electrode-skin impedance of 500 KΩ and α=1.05 for 5% mismatch for dry electrodes

Figure 4.7 Input-referred noise of the proposed AFE with different conditions
The fabricated chip has been tested in EEG eyes-open / eyes-closing experiments. The testing time-domain waveform is shown in Figure 4.8 (a). The corresponding signal spectrum is shown in Figure 4.8 (b), the red line is the spectrum of eyes-closing and blue line is for eye-opening. The peak around 10 Hz of the red line indicates the appearance of α wave when eyes are closing.
Figure 4.8 (a) In-vivo Measurement with eyes open and eyes closed, (b) The corresponding frequency spectrum for eyes open and eyes closed

The performance comparison with other state-of-the-art multichannel EEG AFE designs are shown in Table 4.1. The proposed design achieved a low power consumption per channel of only 1.5 µW. The integrated noise is 0.63 µVrms from 0.5 Hz to 100 Hz, which is the lowest compared to the others. Highest input impedance of 560 MΩ at 50 Hz is achieved with the FIBL. In addition to the 89 dB AFE intrinsic $CMRR_i$, the system-level $CMRR_T$ which is a parameter not reported by the other papers, is 82 dB at 50 Hz and maintained above 80 dB across the frequency range up to 100 Hz.

Table 4.1 Comparison with state-of-the-arts works

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*<sub>CMRR<sub>T</sub> is calculated based on Equation. (15) – (17) with electrode-skin impedance of 500 KΩ and α = 1.05 for 5% mismatch for dry electrodes.

### 4.6 Summary

In this chapter, a 16-channel EEG AFE chip is designed and fabricated in 0.18 µm CMOS technology. A combination of chopping stabilization and time division multiplexing is proposed to achieve high system CMRR, low input noise and low power consumption. A tunable DC-servo loop is inserted to cancel large DC offset from dry electrodes. The proposed 16-channel AFE is a complete design for a typical 10-to-20 system, which can be used for EEG-based HMI in EV applications.
Chapter 5

Design C: An Integrated Multichannel Neural Recording Analog Front-End ASIC with Area-Efficient Driven Right Leg Circuit

5.1 Introduction

Besides EEG-based HMI for EV applications, neural recording technology plays a critical role in brain-machine interface (BMI) applications. The advances in neural sensor electrode and recording circuit development allow the recording of single-unit neuron activity which is essential for advanced neural prosthesis, behavior analysis and therapeutic study [92]. Recent clinical trials have proven the possibility to control prosthetic device by implanting recording electrodes array in the motor cortex area of human brain [93-95]. Techniques such as accurate prosthesis control can be applied to assist the physically handicap individual in the driving of vehicle. But this will require high resolution and high density neural recording, making high performance neural recording circuit design even more challenging.

Recording analog front-end (AFE) is a key building block with stringent design specifications such as input referred noise, power consumption, signal bandwidth and common-mode rejection ratio (CMRR). In general, low input referred noise ensures the signal quality of the recorded neuron activities and low power consumption will extend the lifetime of the implanted recording device in human body. The bandwidth of the neural amplifier should be sufficiently wide to maintain
signal integrity. Moreover, high CMRR is desired to reject strong common-mode interference from AC mains and artifacts. Therefore, a low power (<1 µW), low noise (<5 µVrms) AFE with sufficient CMRR (> 90 dB) and adequate bandwidth (0.5 Hz - 10 kHz) is preferred for neural recording devices.

Figure 5.1 System architecture of an implantable 10-channel neural analog front-end interface

The conceptual system architecture of the proposed multichannel AFE is shown in Figure 5.1. The fully integrated ASIC will be attached to a micro-electrode array and implanted into brain. The neural signal acquired by the electrode array is firstly amplified by a AC-coupled neural amplifier in Stage I. Since the frequency range of neural signal is much wider than EEG signal, which is from 1 Hz to 10 kHz, if
chopping stabilization is used in the design scheme, then the much higher chopping frequency (~tens of kHz) will cause a degraded input impedance of the AFE. Therefore, the TDM/CS technique deployed in Design A and B will not be considered in this design. In design C, an area-efficient capacitor-less DRL block is proposed to average and cancel out the interference signal. The output signals are then multiplexed and digitized by a shared 10-bit SAR ADC in stage II to reduce overall power consumption. Finally, the digitized neural signals are sent out by a wireless transmitter to the external base station.

This chapter is organized as follows: the proposed AFE is introduced in detail with an emphasis on the capacitor-less DRL circuit design in section 5.2. Then the measurement results are presented in section 5.3. Lastly, the conclusions are drawn in summary section.

5.2 System Architecture and Circuit Blocks

The design goal of the proposed AFE is to achieve low-power and low-noise operation simultaneously with high system-level CMRR. Hence, efforts have been focused on the 1st stage amplifier design, where it consists of 10-channels of neural amplifiers and a system-level DRL circuit to cancel the common-mode interference.

A. Area-efficient Driven Right Leg (DRL) Circuit

From Eq. (15) – (17), it is clear that the CMRR₂ mainly depends on the CMRRₑ since the CMRR₁ usually can be more than 90 dB. However, CMRRₑ is easily ruined by impedance mismatch and the reference-sharing effect. For a typical case of a 10-
channel neural-recording system, where with $N = 10$, a safe estimate of mismatch of electrode impedance ($100 \, \text{k}\Omega$) $\alpha$, and input impedance ($500 \, \text{M}\Omega$) $\beta$ is each of 5%. Then both the $\text{CMRR}_E$ and $\text{CMRR}_T$ can be as low as 60dB without any CMRR compensation technique.

Several common-mode compensation techniques, i.e. common-mode feedback (CMFB) [78], common-mode feed-forward (CMFF) [82] and driven right leg (DRL) [79] circuit have been developed to enhance CMRR. For the DRL circuit, the gain setting in the DRL block can degrade the stability performance of the main amplifier. Some advancing methods such as digital-assisted driven right leg (DDRL) [83] and driving right leg (DgRL) [96] have been proposed to improve the performance of the DRL block.

![Diagram of a typical equivalent DRL circuit in biomedical application](image)

Figure 5.2 A typical equivalent DRL circuit in biomedical application [79]

However, various techniques reported in [78] [79] [82] [83] [96] usually requires large passive components for the averaging and coupling of the common-
mode voltage. A typical DRL circuit is shown in Figure 5.2. For a multichannel recording system, the averaging capacitors $C_A$ has to meet the gain requirement:

$$G_{DRL} = N \times C_A / C_{FB}$$  \hfill (20)

then the boosted system-level CMRR, i.e. $CMRR_T$ is defined as:

$$CMRR_T = G_{DRL} \times CMRR_r$$  \hfill (21)

From Equation (20 - 21), it is clear that $CMRR_T$ will be boosted by $G_{DRL}$. To get 40 dB gain for the amplifier in DRL, the value of $C_A$ will be 10 times of $C_{FB}$ for a 10-channel recording system. Base on the typical capacitance density of MIM-capacitor in 0.18 µm CMOS technology, $C_{FB}$ and $C_A$ will require a total area of at least 30000 µm$^2$, which is a significant silicon chip area.

Figure 5.3 The proposed area-efficient DRL circuit with the minimum size $C_A$ in each channel
Therefore, an area-efficient DRL circuit is required to enhance CMRR without significant silicon area overhead. The proposed DRL circuit design is shown in Figure 5.3. The averaging point is changed to the output from the core amplifier in each channel. Hence, \( G_{DRL} \) is defined by the close-loop gain of the recording amplifier itself. Since there is a need to boost the gain in the feedback amplifier in the DRL block, the amplifier \( A_{DRL} \) has been designed as a feedback buffer, which is a capacitor-free structure. Therefore, a minimum area is chosen for the averaging capacitors \( C_A \), to save from the area of the entire recording system. The feedback gain of the DRL circuit can hence be redefined as:

\[
G_{DRL} = \sum_{i=1}^{N} \frac{G_{A_i}}{N}
\]  

(22)

For the proposed 10-channel AFE interface, the selected gain for each instrumental amplifier in stage I and II is 40 dB and 20/16 dB, which is sufficient for DRL block. Comparing with the calculated area for the capacitor in traditional DRL circuit based on the same technology, suppose \( C_{FB} \) is a capacitor of unit size, the original topology requires 101 \( C_{FB} \) for a \( G_{DRL} \) of 40 dB while the proposed new DRL circuit only requires 11 \( C_{FB} \) and hence reducing the area by 90%.

Moreover, since the averaging node of the DRL block is moved from the input of the core amplifier to the output node of the amplifier, the RC pole, which was formed by electrode impedance \( R_E \) and averaging capacitor \( C_A \), is changed to \( R_E C_{IN} \), and pulled further away from the pole formed by the parasitic capacitor (\( C_B \) and \( C_S \)) and electrode impedance \( R_E \). This arrangement will significantly enhance the stability of the core AFE and DRL circuit.
B. Core Recording Amplifier Design

The core recording amplifier adopt a capacitive coupled instrumentation amplifier (CCIA) architecture [92] as shown in Figure 5.4. A current-reuse technique with a pair of input transistor of large W/L is proposed. With this pair of input transistors operating in subthreshold region, high gm efficiency is obtained to suppress the flicker noise within the low frequency range from 1 Hz to 10 kHz for neural recording, and two pseudo-resistors are used for the common mode feedback in the second stage of the amplifier. The current consumption of the core amplifier is only 1 µA, with a supply voltage of 1 V.

Figure 5.4 Schematic of the proposed two-stage fully differential amplifier with current-re-use technique
The schematic of the differential-to-single buffer in stage-II is shown in Figure 5.5, the gain setting (14/20 dB) is controlled by the voltage of GAIN, while the bandwidth of the buffer is controlled by the current consumption by applying different voltage (0/1.8 V) to BW. Therefore, the amplifier in stage-II have high/low gain settings and HP/LP bandwidth settings as well.

Figure 5.5 (a) Schematic of the closed-loop differential-to-single amplifier with high/low gain setting, (b) Schematic of the core amplifier with HP/LP setting

The schematic of the 9-bit SAR ADC is shown in Figure 5.6 (a), which consists of four blocks: a time-domain comparator, a switch array, a capacitor bank and a logic control block. Ten analog signals from all the channels are sent into the 9-bit ADC and digitized to be serial-output. The time diagram is shown in Figure 5.6 (b), a dual S/H structure is implemented in this ADC, when the signal from channel 1 is in conversion phase, the signal from channel 2 is in sampling phase.
Figure 5.6 (a) Schematic of the 9-bit SAR ADC, (b) Timing diagram of the dual S/H structure

5.3 Measurement Results

A 10-channel neural recording AFE test chip has been designed in a standard commercial 0.18-μm 1P6M CMOS process. The die photo of the AFE chip is shown in Figure 5.7. The area of the overall active circuit and each channel are 1.65 mm² and 0.09 mm², respectively. Figure 5.8 shows the measured results of AFE frequency response under high/low gain settings. The high pass corner is 0.26 Hz and 0.15 Hz for high/low gain respectively while low pass corner is 9.4 kHz and 12.1 kHz. The AC response of two bandwidths settings is shown in Figure 5.9. For high-pass mode,
the low cutoff frequency is 820 Hz, and for low-pass mode, the high cutoff frequency is 1.3 kHz.

The input-referred noise of the proposed AFE interface is given in Figure 5.10, which is only 20 nV/sqrt (Hz) and 4.6 µVrms, integrated from 1 Hz to 10 kHz at high gain mode. Since the bandwidth of the neural signal is much wider than EEG signal, chopping stabilization is not applied to the structure of this IA. Hence, flicker noise density of the IA in this design is much higher than the IA used in design A and B within low frequency range (0.5 – 100 Hz). An in-vivo testing for ECG measurement is implemented to verify the functionality of the DRL circuit. The output of the proposed AFE both with and without the proposed DRL circuit is shown in Figure 5.11 for comparison. It can be observed that, when DRL is off, the AFE output is saturated by the 50 Hz common-mode interference signal. When DRL is on, the system CMRR is further boosted by 60 dB, so that the interferences are effectively suppressed. The current consumption for each channel is only 1 µA at 1 V supply voltage. The performance comparison with the other state-of-the-art designs is shown in Table 5.1. 90% chip area reduction is achieved compared to the architecture used in [99].

![Die photo of the proposed 10-channel AFE](image-url)
Figure 5.8 The frequency responses of two gain setting (60dB /54dB) of the proposed AFE

Figure 5.9 The frequency responses of two bandwidths setting (HP/LP) of the proposed AFE
Figure 5.10 The input-referred noise density of the proposed AFE

Figure 5.11 The measured output of a real ECG signal from the AFE with/without DRL circuit for comparison
Table 5.1 Performance summary and benchmark table

<table>
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<td>1</td>
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<td>1</td>
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</tr>
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<td>32</td>
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*estimated from die photo

5.4 Summary

A 10-channel neural recording AFE with an area-efficient DRL circuit is designed in a 0.18-µm CMOS technology. The novel area-efficient DRL circuit is able to reduce the capacitor area by 90% compared to the conventional DRL circuits. The proposed AFE has a bandwidth of between 0.26 Hz to 9.4 kHz. It achieves noise performance of 4.6 µVrms at 1 µW power consumption. Therefore, the proposed design is suitable for neural recording system for BMI in EV applications.
Chapter 6

Design D: A Bio-potential Recording Analog Front-End ASIC with Enhanced Power Efficiency Factor

6.1 Introduction

In order to design a ExG-based HMI for driver’s daily health status monitoring in EV applications, the hardware resources of recording system and power consumption should be miniaturized, a highly-integrated bio-potential AFE is designed to record both the ExG signals and neural LFP and AP signals. Because the ExG signals and LFP are mainly located within 0.5 Hz to 1 kHz while the AP spikes are usually in the range of 500 Hz to 7.5 kHz, the bandwidth of the AFE should be larger than 10 kHz. Since these bio-potential signals’ amplitude varies from 1 µV to several mV, the AFE is designed with programmable gains. And the flicker noise can easily ruin the ExG signals which are within low frequency range, a chopping-stabilization scheme is lunched to improve noise performance and ensure optimal signal quality of the ExG signals.

Two TDM-based AFE is proposed in Chapter III and IV for EEG-based HMI. A neural recording AFE with area-efficient DRL is then developed for BMI in Chapter V. In this chapter, a bio-potential recording AFE ASIC with enhanced Power Efficiency Factor (PEF) for ExG-based HMI in EV applications is described. A high frequency chopping technique is applied to ensure low noise within a wide
bandwidth from 0.5 Hz to 10 kHz. A pair of off-chip de-coupling capacitor is used to achieve rail-to-rail DC cancellation. The impedance boosting loop compensates the impedance loss due to chopping modulation.

6.2 System Architecture and Circuit Block

The system architecture is shown in Figure 6.1. The proposed system consists of a CS-CCIA and a programmable-gain low-pass filter (LPF). The gain of the CCIA and LPF are 40 dB and 16/20 dB, respectively. This bio-potential AFE design mainly focuses on three issues: 1) power efficiency; 2) noise performance; 3) DC offset cancellation, which are conducted in the following analysis.

![System architecture of the proposed bio-potential recording AFE](image)

Figure 6.1 System architecture of the proposed bio-potential recording AFE

1) Power Efficiency

Some previous work [106] discussed about the tradeoff between noise and power, and introduced noise efficiency factor (NEF) to quantifies this tradeoff. The NEF is defined as:
\[ \text{NEF} = V_{\text{ni,rms}} \sqrt{\frac{2I_{\text{tot}}}{\pi gU_T g^4 kT gBW}} \]  

(23)

where \( V_{\text{ni,rms}} \) is the input-referred noise and \( I_{\text{tot}} \) is the total current consumption, \( U_T \) is the thermal voltage \( kT/q \) and \( BW \) is the bandwidth of the AFE. In an ideal case, an amplifier with single bipolar transistor has an NEF equals to 1.

However, the NEF only deals with current consumption and noise performance for amplifiers. It is unfair to use NEF for comparison between two amplifiers with different supply voltage. Some work [107] proposed a new parameter, power efficiency factor (PEF), which introduced supply voltage into the equation (23) to evaluate the tradeoff between power and noise performance more accurately. PEF is defined as:

\[ \text{PEF} = \text{NEF}^2 \frac{V_{DD}^2}{g_{DD}^2} = V_{\text{ni,rms}}^2 \left( \frac{2P_{\text{tot}}}{\pi gU_T g^4 kT gBW} \right) \]  

(24)

where \( P_{\text{tot}} \) is the total power consumption of the proposed circuit block.

With advanced CMOS technology, threshold voltage of a transistor can be further reduced. Hence, supply voltage of the AFE circuit can be scaled down to pursue ultra-low power operation for long-term monitoring systems. By using the low-Vth devices in UMC 65nm technology, the supply voltage of our previous design is scaled from 1V to 0.5 V. Therefore, with the same NEF performance, the PEF of the proposed design will drop by 50%, which is a great enhancement for power efficiency. Although the leakage current of the low-Vt device in advanced process is higher than the conventional device in 0.18 µm CMOS process, with
chopping stabilization, the noise performance will still be optimal with scaled power supply. Considering the signal amplitude and gain settings of the proposed AFE, 0.5 V is an optimal choice for supply voltage since further scaling of the supply voltage will saturate the bio-potential signal at the output terminal of the proposed AFE.

2) Noise Performance

For various bio-potential recording applications, there are different design strategies for low noise amplifiers. For example, because EEG signals are mainly in the frequency range from 0.5 Hz to 100 Hz, which suffers a lot from flicker noise, the EEG recording amplifier usually requires chopping stabilization to modulate the flicker noise. While the neural recording amplifier usually deploys large size transistor to suppress the flicker noise since the frequency of the neural AP is much higher than EEG signals. However, our design target is to develop a low-noise bio-potential AFE for both ExG and neural applications. A general chopping-stabilization scheme for EEG applications has a chopping frequency between 2 kHz to 4 kHz [85] [86] [89] [91], which is in the frequency range of neural AP signals. If such low frequency chopping scheme is applied to the proposed design, there will be many ripples located at the combinational frequency of chopping signals and neural signals. Therefore, for our bio-potential AFE, a high-frequency \( f_{CH} = 20 \) kHz chopping-stabilization scheme is implemented to avoid signal mixing. Moreover, for the compensation of input impedance loss due to chopping-stabilization, an impedance boosting loop is applied to the CS-CCIA block.

3) DC Offset Cancellation
When chopping-stabilization is used in the front-end circuit, one serious problem is the dc offset between two electrodes will be modulated into the amplifier, the large offset, as high as serval hundreds of mV, saturates the output of the front-end. DC-servo loop is a popular tool for dc offset cancellation. However, the negative offset feedback path will introduce extra noise to the inputs of the core amplifier. The amount of the coupled noise from the DC-servo loop is proportional to the value of the coupling capacitor, or in another way, the amount of the cancelled DC offset. Therefore, there is a tradeoff between noise performance and the capability of DC offset cancellation when DC-servo loop is implemented in the front-end designs.

Another way to cancel the DC offset is to put de-coupling capacitor in front of the chopping switches. However, the value of the de-coupling capacitor should be large enough compared with the input coupling capacitors to avoid gain mismatch. If the de-coupling capacitor is put on-chip, the size of the capacitors will occupy huge chip area. Therefore, off-chip de-coupling capacitors is selected for our area-efficient AFE design to achieve rail-to-rail DC offset cancellation.

6.3 Simulation Results

The proposed low-power low-noise bio-potential AFE with enhanced PEF is designed in UMC 65nm technology. The chip was sent out for fabrication in April 2017, and is pending for further testing. The layout of the chip is shown in Figure 6.2, and the area of the chip is only 0.176 mm².
As shown in Figure 6.3, the AC response for two gain selections are 54 dB/60dB while the low cutoff and high cutoff frequency are 0.6 Hz/11.4 kHz for high gain mode and 0.3 Hz/19.8 kHz for low gain mode.

The noise performance is shown in Figure 6.4, with the help of high-frequency chopping, the noise density is only 21nV/\sqrt{Hz}). The input-referred noise is only 2.05 \mu V_{\text{rms}} integrated from 1 Hz to 10 kHz.

The pre-recorded ECG signal and neural signal are sent in for bio-signal simulation and the output of the proposed AFE is shown in Figure 6.5.
parts of the ECG signal and the neural spikes are quite clear and suitable for data analysis.

Figure 6.4 Input-referred noise of the proposed AFE design

Figure 6.5 The simulated output of the proposed AFE according to the pre-recorded (a) ECG signal and (b) neural signal
The comparison of the proposed bio-potential AFE design with the-state-of-the-art work is carried out in Table 6.1. Under the supply voltage of 0.5 V, our design has a power consumption of 2 µW. By using the high-frequency chopping stabilization technique, the integrated input referred noise is only 0.18 µVrms from 1 Hz to 100 Hz, and 2.1 µVrms from 1 Hz to 10 kHz, both of which are the lowest for the comparison on noise performance among the other work. Our design has achieved the smallest NEF and PEF when comparing with other works.

Table 6.1 Comparison with the-state-of-the-arts works

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<td>45-65</td>
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<td>7 (200Hz-5KHz)</td>
<td>4.13 (1Hz-8.2kHz)</td>
<td>0.58 (0.5Hz-500Hz)</td>
<td>7.5 (100Hz-10KHz)</td>
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*post-layout simulation results
6.4 Summary

In this chapter, a low-power, low-noise bio-potential recording AFE is proposed with enhanced PEF performance. The AFE has obtained the smallest PEF of 1.3 under 0.5 V supply voltage with power consumption of 2 µW. Integrated input-referred noise of the AFE is only 2 µVrms with high-frequency chopping scheme. Rail-to-rail DC cancellation is achieved by off-chip de-coupling capacitors. This AFE is suitable for EEG, ECG, EMG, and neural signal recording. Therefore, the proposed bio-potential AFE can be used for ExG-based HMI in EV applications.
Chapter 7

Conclusion and Future Work

7.1 Conclusions

In this thesis, four low-power, low noise, high CMRR analog front-end for wearable HMI in EV applications were proposed. For wearable EEG recording system, one of the major concern is the system-level CMRR. Since common reference montage is widely used for EEG recording front-end, the reference input is shared by all channels, and the imbalance load of the two inputs causes degradation of CMRRI and CMRRT. Several techniques such as CMFF, CMFB and DRL block had been reviewed in this thesis.

The TDM-based analog front-end in chapter three focuses mainly on the improvement of system-level CMRR improvement. A four-channel TDM-based analog front-end is proposed as a prototype for wearable HMI in EV application. The time division multiplexing technique is combined with chopping stabilization to reduce the number of sharing channels to one and at the same time suppress flicker noise. The fabricated analogue front-end achieved a system-level CMRR of more than 80 dB with a typical value of electrode impedance and electrode mismatch. The chop/mux analog front-end obtains an optimal noise performance of 0.72 μVrms integrated from 0.5 Hz to 100 Hz while the power consumption for the entire system is 5 μW with a power of 1.25 μW per channel.
The TDM-based analog front-end achieves enhanced system-level CMRR but four channels are insufficient for some wearable EEG applications. A second design, which is a 16-channel TDM analog front-end, is thus proposed in chapter IV as the most representative design among the four designs with enhanced CMRR, tunable DC-servo loop and calibratable impedance boosting loop. The proposed design achieves a low power consumption per channel of only 1.5 µW. The integrated noise is 0.63 µVrms within 0.5 Hz to 100 Hz, which is the lowest compared to the state-of-the-arts work. The highest input impedance of 560 MΩ at 50 Hz is achieved with the FIBL. In additional to the 89 dB AFE intrinsic CMRR, the system-level CMRR, which is a parameter not reported by the other papers, is 82 dB at 50 Hz and it remains above 80 dB across the frequency range up to 100 Hz.

Besides the TDM-based CMRR improvement technique i.e., the proposed area-efficient DRL circuit is introduced for CMRR enhancement as the third design in chapter five. A 10-channel neural recording AFE with an area-efficient DRL circuit is designed using 0.18-µm CMOS technology. The novel area-efficient DRL circuit which feedbacks the large common mode signal from the output of each channel, is able to reduce the capacitor area by 90% compared to the conventional DRL circuits. The proposed AFE has a bandwidth of between 0.26 Hz to 9.4 kHz. It achieves noise performance of 4.6 µVrms at 1 µW power consumption, making it suitable for a multichannel neural recording system.

Another problem for biopotential recording analog front-end is the noise efficiency. PEF is considered as a more accurate parameter for evaluation of the tradeoff between power consumption and noise performance. The fourth design
which focuses on PEF enhancement is proposed in chapter six. The AFE obtains the smallest PEF of 1.3 under 0.5 V supply voltage, with a power consumption of 2 \( \mu W \). The integrated input-referred noise of the AFE is only 2 \( \mu V_{\text{rms}} \) with high-frequency chopping scheme. The rail-to-rail DC cancellation is also realized using off-chip de-coupling capacitors. Therefore, the proposed AFE is suitable for bio-potential recording system.

7.2 Future Work

There is still much work to be done in the area of EEG recording front-end design. With the development of CMOS technology, EEG recording chip heads towards greater energy-efficiency, lower noise and higher density system with more functionalities. Therefore, some perspectives can be addressed here for future work.

7.2.1 Electrode Tissue Impedance Monitoring

Electrode-tissue impedance (ETI) is considered an important parameter for the EEG recording system, especially for wearable EEG devices. An ETI measurement block should be integrated with the front-end interface for impedance monitoring during long-term recording.

As shown in Figure 7.1, the ETI signal is measured by injecting the up-modulated current into human body through the recording electrode. Thereafter, the ETI current is translated into ETI voltage with an up-modulated frequency. Therefore, the EEG and ETI signal are separated and can be recorded by the recording front-end, simultaneously. The DC-coupled EEG analog front-end [73]
shall use a low-pass filter for the removal of ETI from the EEG signals. With the help of ETI measurement, the electrode CMRR, i.e. CMRR$_1$ of EEG acquisition system can be real-time monitored. Moreover, any electrode movement or motion artifacts will be detected by the ETI measurement block.

![Figure 7.1 Schematic and signal spectrum of EEG/ETI measurement [73]](image)

### 7.2.2 Chopping Ripple Reduction

Chopper stabilization reduces the flicker noise in baseband, but the chopping ripple is considered additional noise for EEG front-end interface. A ripple reduction loop (RRL) [111] solves this problem by implementing a feedback path to remove the ripples. This is an efficient way to ensure quality of EEG signal although the loop consumes extra power.
Figure 7.2 A simplified AC-coupled ripple reduction loop [111]

As shown in Figure 7.2, the output ripples voltage is sensed and converted into ripple current by the capacitor $C_4$. The ripple current $I_{AC}$ is then modulated by the chopper CH$_6$ to be a DC current $I_{DC}$. The $C_{int}$ and $G_{m6}$ integrates the DC current and the integrated voltage $V_o$ is fed into the output $G_{m3}$ and $G_{m4}$ for ripple compensation.

Another approach to reduce the ripple is to spread the ripple energy over a large spectrum range. When a pseudo-random chopping scheme [112] is applied to the instrumentation amplifier, since the chopping frequency varies from 50 to 150 kHz, the spectrum of chopping ripples will be spread across a bandwidth of 100 kHz. After which the ripples can be easily filtered-out by a low-pass filter. One major concern for this method is the complicated pseudo random clock generation. In [112], the random chopping clock is generated from a 15 MHz clock with a repetition cycle of 80 seconds.
7.2.3 Self-adaptive DC Cancellation

Previous work on DC cancellation technique had focused on the capability of maximum DC offset cancellation. However, the DC servo loop works as a time-consuming feedback path which may takes more than 1 hour for about 300 mV offset cancellation. Some work [86] proposed fast-settling DC-servo loop by controlling the resistance of pseudo resistor, while the reported DC-servo loop can only be calibrated between two settling modes. Moreover, the electrode offset changes with time while the previous DC-servo loop cannot be adapted to response to the change of the electrode DC offset. Therefore, a self-adaptive DC cancellation loop is required to be implemented in the chopping stabilized instrumentation amplifier proposed in this thesis.

Figure 7.3 schematic of CS-CCIA with self-adaptive DC-servo loop [91]
As shown in Figure 7.3, a self-adaptive DC-servo loop is included in the CS-CCIA of the EEG recording front-end. The output voltage will be sensed and sent into the ARU block to determine the applied gate voltage of the pseudo-resistors $R_{psu2}$. If the input DC offset saturates the output of the amplifier, the ARU block will lower the gate voltage of the pseudo-resistors. This method can achieve self-adaptive DC cancellation, the response speed is still limited by the 4-bit comparator in the ARU block. Some work [113] has proposed a new mix-mode DC-servo loop (MM-DSL) with a digital DSL for wide range DC cancellation and an analog DSL for fine resolution. By implementing the two DSL in the AFE simultaneously, the AFE can cancel 100 mV DC offset within 130 ms.
Appendix

Derivation of CMRR$_T$ and CMRR$_E$

For multi-channel recording front-ends, the system-level CMRR is an important parameter to evaluate the capability of common mode rejection. For the system-level CMRR, i.e. CMRR$_T$ is derived as equation (15). For a wearable biopotential recording system, the CMRR of the input interface, i.e. CMRR$_E$ is usually smaller than the intrinsic CMRR, CMRR$_I$. Therefore, CMRR$_T$ usually depends on CMRR$_E$.

For a multi-channel recording front-end, the equivalent model of a is shown in Figure A.1. $Z_E$ is the electrode impedance and $Z_{IN}$ is the input impedance of the amplifier, $N$ is the number of sharing channels and $\alpha$ is the impedance mismatch between two electrodes.

![Equivalent circuit model for a single channel EEG AFE in a multichannel recording system. The negative inputs of all channels are tied together and connected to the reference electrode.](image)

Figure A.1 Equivalent circuit model for a single channel EEG AFE in a multichannel recording system. The negative inputs of all channels are tied together and connected to the reference electrode.
$CMRR_E$ is defined by the ratio of $G_{DD}$ to $G_{CD}$, where $G_{DD}$ is the differential mode gain defined as ratio of differential mode output to differential mode input:

$$G_{DD} = \frac{V_{difOUT}}{V_{difIN}} = \frac{Z_{IN}}{2Z_E} \left( \frac{1}{\left| \frac{Z_{IN}}{Z_E} \right| + 1} + \frac{1}{\left| \frac{Z_{IN}}{Z_E} \right| + N\alpha} \right) \quad (A.1)$$

$G_{CD}$ is the common mode gain defined as the ratio of common mode output to common mode input:

$$G_{CD} = \frac{V_{cmnOUT}}{V_{cmnIN}} = \frac{Z_{IN}}{Z_E} \left( \frac{1}{\left| \frac{Z_{IN}}{Z_E} \right| + 1} - \frac{1}{\left| \frac{Z_{IN}}{Z_E} \right| + N\alpha} \right) \quad (A.2)$$

Therefore, the $CMRR_E$ is defined as:

$$CMRR_E = \frac{G_{DD}}{G_{CD}} = \frac{1 + 2\left( \left| \frac{Z_{IN}}{Z_E} \right| \right) + N\alpha}{2(N\alpha - 1)} \quad (A.3)$$

Then the $CMRR_T$ is derived as:

$$CMRR_T = \left( CMRR_E^{-1} + \frac{2(N\alpha - 1)}{1 + 2\left( \left| \frac{Z_{IN}}{Z_E} \right| \right) + N\alpha} \right)^{-1} \quad (A.4)$$
Publications


6. **Tao Tang**, Wang Ling Goh, Lei Yao, Jia Hao Cheong and Yuan Gao. “An Integrated Multichannel Neural Recording Analog Front-End ASIC with Area-
Efficient Driven Right Leg Circuit,” *IEEE Transaction on Circuit and System II (TCAS-II)*, 2017. (To be submitted)
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