DESIGN OF POWER MANAGEMENT CIRCUITS FOR FULLY ON-CHIP APPLICATIONS

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING
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Abstract

With the fast growing electronic portable devices, power management becomes an important area in electronic industry to reduce the power consumption so as to extend the battery life of these devices. Low dropout (LDO) regulator is widely used in power management IC due to its simple structure, low noise and fast speed characteristics. As the technology continues scaling down to deep submicron, the digital circuits display less immunity to Process, Supply voltage, and Temperature (PVT) variations. Therefore, power management technique with PVT compensation becomes another important design approach. This work focuses on the design techniques which include process variation sensing circuit ($V_{\text{TH}}$ sensor), wide load capacitance ($C_L$) range with fast speed LDO regulators and digital system supply with PVT compensation capability using LDO regulator.

First, the $V_{\text{TH}}$ sensor circuit can generate the $V_{\text{TH}}$ of a single MOSFET at 0 K ($V_{\text{TH0}}$). $V_{\text{TH0}}$ is temperature and supply invariant but process dependent. The $V_{\text{TH}}$ sensor can be utilized to sense the $V_{\text{TH}}$ variation of the devices, hence providing the process information. Based on a Brokaw structure with the addition of the proposed current-mode second-order temperature compensation network, this improves the Temperature Coefficient (T.C.), the $V_{\text{TH}}$ sensor.

Second, a DSMFC technique is proposed in a Flipped Voltage Follower (FVF) LDO regulator architecture. By adding an extra Miller compensation stage, the dominant pole of the feedback system can be pushed to lower frequency whilst the non-dominant pole(s) can be pushed to higher frequency. This extends the $C_L$ driving range without sacrificing circuit complexity and quiescent power consumption.
Third, a novel Weighted Current Feedback (WCF) technique is proposed in a multi-gain stage LDO regulator architecture. Through feedback of a weighted current, the WCF permits smart management of the output impedance as well as the gain from the inter-gain stage. As a result, a good optimization of stability, speed and accuracy can be achieved in the context of wide $C_L$ range.

Finally, a PVT Compensated Supply (PVTCS) for driving point-of-load digital system is designed. By adding a weighted combination of the $V_{TH}$ drift of the PMOS ($\Delta V_{THP}$) and NMOS ($\Delta V_{THN}$) diodes onto the reference voltage of a high speed WCF LDO regulator, the supply voltage of the digital circuits is adjusted adaptively. This can reduce the speed deviations of the digital circuits under PVT variations.

With the low T.C. $V_{TH}$ sensor circuit to sense the process information, the two wide $C_L$ range LDO regulators to drive the digital circuits and the PVTCS to compensate the PVT variations of the digital systems, the works are useful for fully on-chip power management circuits with PVT compensation.
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<th>Full Form</th>
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<tr>
<td>BBG</td>
<td>Body Bias Generator</td>
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<td>BGR</td>
<td>Bandgap Reference</td>
</tr>
<tr>
<td>CG</td>
<td>Current Generator</td>
</tr>
<tr>
<td>CTAT</td>
<td>Complementary-to-absolute-temperature</td>
</tr>
<tr>
<td>Cox</td>
<td>Gate oxide capacitance</td>
</tr>
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<td>D2D</td>
<td>Die-to-Die</td>
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<td>DDA</td>
<td>Differential Difference Amplifier</td>
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<td>Low Dropout</td>
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<td>Monte-Carlo</td>
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<td>NBG</td>
<td>Negative Bias voltage Generator</td>
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<td>NCF</td>
<td>Negative Current Feedback</td>
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<td>OC-LDO</td>
<td>Output Capacitor LDO</td>
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<td>OCL-LDO</td>
<td>Output Capacitorless LDO</td>
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<tr>
<td>OTA</td>
<td>Operational Transconductance Amplifier</td>
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<tr>
<td>PCB</td>
<td>print-circuit-board</td>
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<td>PM</td>
<td>Phase Margin</td>
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<td>Power Supply Rejection</td>
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<td>PTAT</td>
<td>Proportional To Absolute Temperature</td>
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<tr>
<td>PVTCS</td>
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<td>RHP</td>
<td>Right-Half-Plane</td>
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<td>Ron</td>
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<td>$V_{DS}$</td>
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<td>$V_T$</td>
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<td>$T_r$</td>
<td>Room temperature ($T_r = 300$ K)</td>
</tr>
<tr>
<td>$\kappa$</td>
<td>T.C. of $V_{TH}$</td>
</tr>
<tr>
<td>$m$</td>
<td>Mobility temperature exponent whose typical value is 1.5 for CMOS</td>
</tr>
</tbody>
</table>
CHAPTER 1

INTRODUCTION

This Chapter gives the motivations, objectives, and contributions of this research work.

1.1 Motivations

With the fast growing electronic portable devices, power management becomes an important area in electronic industry to reduce the power consumption so as to extend the battery life of these devices. A power management circuit (IC) normally comprises switching regulator, linear regulator and power control logic [1]. The control logic inside the power management IC is normally used to control the power delivery to the loading circuit.

For the switching regulator, due to the switching nature, it can support AC-AC, AC-DC, DC-AC and DC-DC conversions. In the context of ICs, DC-DC converter predominates because the ICs normally derive power from the dc batteries and other dc supplies [1]. Figure 1.1(a) shows the most popular scheme among the DC-DC converters which employs the pulse width modulation (PWM) technique. A linear error amplifier compares the feedback output voltage with the reference voltage. Through a PWM converter, the error amplifier output voltage is converted into a digital switching signal having different duty ratios to drive the power transistors. Finally, a low power filter is applied on the digital switching waveform and a DC voltage can be generated. Due to the switching operation characteristics, the DC-DC converter can generate wide range of output voltages, including voltage below (buck converters [2-4]), above (boost converter [5-7]) and above-or-below (buck–boost...
converter [8-10]). Since the voltage across the power transistor in DC-DC converter are small (10 mV – 100mV), above 80% power efficiency can be achieved. However, the output noise is high because of the on-off switching in the power transistors. Finally, due to the external large inductor and capacitor which are using to form the low pass filter, the DC-DC converter hardly supports full integration with the load circuits.

Regarding the linear regulator, as shown Fig. 1.1(b), the error amplifier output voltage directly drive the power transistor and control its on-resistance instead of converting into digital signals. Since the current in the power transistor is continuous in time, the circuit is linear and analog in nature. The resulting output voltage has lower noise with respect to the DC–DC converter. However, the output voltage of linear regulator cannot exceed the input supply voltage. In addition, the voltage drop across the series switch in the linear regulator is normally larger than 0.2 V which limits its conversion power efficiency. Lastly but most importantly, the linear regulator can be designed with and without off-chip capacitors. They are named as the output-capacitor based linear regulator and the output capacitorless liner regulator, respectively. For output capacitorless linear regulator, it is possible to fully integrate it

![Fig. 1.1: (a) PWM switching regulator structure. (b) Linear regulator structure. [1]](image-url)
with loading circuits which can reduce the cost by using less number of I/O pins, less
print-circuit-board (PCB) area and less external components.

Table 1.1 compares the performance of switching regulator and linear regulator. As indicated in this table, the switching regulator can provide a wide range of output voltages and benefit from having high power efficiency while show large noise on the output voltage. On the other hand, the linear regulators exhibit limited power efficiency due to its quiescent current flow and the large input-to-output voltage difference across the power transistor. However, the linear regulator can give stable and low noise output voltage whilst offering the fully on-chip capability. It is therefore suitable for modern System-on-Chip (SoC) applications [11-15].

<table>
<thead>
<tr>
<th>Linear Regulators</th>
<th>Switching Regulators</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output range is limited ($V_{OUT} &lt; V_{IN}$)</td>
<td>√ Output range is flexible($V_{OUT} \leq \text{ or } V_{IN}$)</td>
</tr>
<tr>
<td>□ Simple circuit</td>
<td>Complex circuit</td>
</tr>
<tr>
<td>□ Low noise content</td>
<td>High noise content</td>
</tr>
<tr>
<td>□ Fast response</td>
<td>Slow response</td>
</tr>
<tr>
<td>Limited power efficiency ($\eta &lt; V_{OUT}/V_{IN}$)</td>
<td>√ High power efficiency ($\eta \approx 80%\text{–}95%$)</td>
</tr>
<tr>
<td>Good for low-power applications</td>
<td>Good for high-power applications</td>
</tr>
<tr>
<td>□ Can be fully integrated with loading circuit</td>
<td>Normally stand-alone</td>
</tr>
</tbody>
</table>

LDO regulators belong to the linear voltage regulators with improved power efficiency by reducing the differences between the input voltage $V_{IN}$ and the output voltage $V_{OUT}$. Due to the improved power efficiency and fast speed characteristics, LDO regulator can be utilized to drive the subsystem of the ICs including point-of-load digital circuits [16] and analog/mixed-signal blocks. Under low supply voltage environment, the digital circuits normally consume low to moderate power but the currents are fast switching. Besides, the parasitic capacitance at the supply line can be
large due to the large number of transistors connected to the supply line. As such, the LDO regulator to drive such circuit needs to have a wide load capacitance ($C_L$) driving ability with fast transient responses.

There are two categories for LDO regulator as well. They are output capacitor based LDO regulator (OC-LDO) and output capacitorless LDO (OCL-LDO) regulator. For OC-LDO regulator, it relies on a μF level off-chip capacitor to maintain stable operation. The off-chip capacitor can source and sink current during load switching which can reduce the transient overshoot and undershoot. However, it also limits the fully integration ability of LDO regulator. On the contrary, the OCL-LDO regulators [17-34] have received much attention recently since it eliminates the output capacitor through using internal compensation to achieve stability. The load capacitance $C_L$ of the OCL-LDO regulator is then purely formed by the parasitic capacitance on the supply line of loading circuit which is normally from few ten pF to few nF range. The OCL-LDO regulators are widely used for on-chip applications for modern SoCs. For first example, the linear regulator, which is powered by switching regulators, delivers the current to sub-blocks of the system that requires low noise and stable supply voltage like LNA, frequency synthesizer, Mixers in cellular phones and PDA (personal digital assistant) [35, 36]. For second example, to implement fine-grain on-chip power domains or dynamic-voltage-scaling (DVS) [26], multiple on-chip LDO regulators are required to drive the sub-blocks (like memory banks, DSPs). Figure 1.2 depicts a typical structure of a switching regulator driving few LDO regulators in a power management system [37]. It can be seen that the OCL-LDO regulator is an essential building block in SoC IC.
Though the OCL-LDO regulator offers fully on-chip merit with respect to the OCL-LDO regulator, the design challenges are increased in the OLC-LDO regulator. These are summarized as follows. First, without the large output capacitor to source or sink current, the undershoot and overshoot of OCL-LDO regulators are normally much larger than the OC-LDO regulator counterpart. To improve the transient performance, the adaptive biasing technique \[25, 27\] has been reported to dynamically increase the biasing current of the error amplifier, hence increasing the loop gain-bandwidth product. However, due to a positive feedback loop exists in the adaptive feedback loop, it is difficult to control the stability. Direct voltage spike detection technique \[23\] senses the output voltage spike and generates a spike current to charge or discharge the gate of power transistor and the output node with improved speed. Unfortunately, the structure is limited by the small feedback loop gain. More importantly, poor regulation accuracy is obtained due to its single-stage amplifier topology.

Second, to ensure regulation accuracy, a multi-gain stage amplifier topology is typically employed to drive the power transistor. Under low quiescent current constraint, the output impedances of the gain stages are high, leading to several low frequency poles. In order to achieve stability, some appropriate frequency

Fig. 1.2 A typical SoC IC with power management unit [37].
compensation techniques should be applied. For a standard Miller compensation, the required compensation capacitor $C_m$ is proportional to the load capacitor $C_L$. For a large $C_L$, $C_m$ will be large, thus contributing large silicon area. Moreover, a large $C_m$ will also result in small gain bandwidth product (GBW), reducing the speed of LDO regulator. This in turn increases the design difficulty of the OCL-LDO regulator, especially for applications with wide range of $C_L$. Therefore, in most of the reported OCL-LDO regulator designs, they usually drive a maximum $C_L$ up to tens of pF or 100 pF [21, 22, 24, 27, 28, 30]. Few designs can drive relatively large $C_L$ [18, 23, 26, 29, 34]. Figure 1.3 depicts the maximum $C_L$ versus quiescent current for reported state-of-the-art OCL-LDO regulators. It can be observed that under low quiescent current constrains, most of the reported works can only drive small $C_L$. This may not be useful for the SoC environment having large scale digital circuits. As a result, the effective supply line parasitic capacitance becomes very large. To drive such the circuits, the LDO regulator should have the ability to drive a wide $C_L$ range (few hundred pF to few nF) [38].

With the above mentioned design challenges in the OCL-LDO regulators, in this research work, OCL-LDO regulator topologies and circuit techniques which can drive wide range of $C_L$ with fast transient responses are explored.

To drive large scale digital circuits, the power management system needs to be well controlled in order to save power without affecting the circuit performance. A popular driving scheme is the dynamic voltage frequency scaling (DVFS) [39, 40]. Based on different workloads, computation conditions or objective functions, the supply voltage of the circuit is reduced when performance constrains are relaxed. For example, most DVFS-based mobile and embedded devices typically spend the majority of their lifetimes in operating in low-power mode [41]. Figure 1.4 depicts a
Fig. 1.3: Maximum load capacitance versus quiescent current for the reported OCL-LDO regulators.

Fig. 1.4: A sample of power and ground plan of microprocessor [42].
sample of power and ground plan using DVFS technique [42]. Though the DVFS can reduce the power consumption of digital circuits, the supply voltage is still fixed under normal operating condition. The may lead large speed deviation if nanometer technology with large process variation is used. This is given and discussed as follows:

As CMOS technology continues to scale down, transistors parameters including threshold voltage ($V_{TH}$), channel length, oxide thickness and mobility depicts large process variations [43, 44]. In addition, the environmental temperature variations change the mobility of the electrons and holes whilst modifying the $V_{TH}$ of the devices, thereby causing the circuit speed variations [43, 45, 46]. Furthermore, the supply voltage $V_{DD}$ is another critical parameter that directly affects the transient current of the digital circuits because the saturation current of the transistor is proportional to $\alpha/(V_{DD}-V_{TH})$, where $\alpha$ is the carrier mobility degradation factor [45, 47]. Through summing up these effects, the digital system will exhibit a wide deviation of performance under process, voltage and temperature (PVT) variations, particularly significant in nanometer CMOS technologies.

Of another concern, with the tremendous increase in portable electronic devices, the reduction of power consumption in digital Large-Scale Integration (LSI) becomes an important matter to extend the battery life. The most effective and direct way is to reduce the power supply voltage ($V_{DD}$) due to the square law relation between the power consumption and $V_{DD}$ [45, 48]. However, when $V_{DD}$ comes close to the threshold of transistor ($V_{TH}$), a small variation of PVT will result in the significant degradation of chip performance [49]. Figure 1.5 illustrates the CMOS digital circuit’s delay and power parameters fluctuates with respect to $V_{DD}$ [48]. As can be seen from the graphs, both the key parameters substantially increase when the $V_{DD}$ scales down.
To reduce the performance deviation of the digital circuits or improve the yield, for the fixed supply system using DVFS, the minimum supply voltage is chosen on the basis of the worst case corners (process and temperature). This may waste a lot of power since some of the function blocks may not need such high supply voltage. The speed of the digital circuit will also vary significantly under process variations. Another technique is to implement PVT compensation during design process. Under different process and temperature conditions, the supply voltage of the digital system is dynamically varied to reduce the variation of speed.

Figure 1.6 depicts the generic block diagram in an exemplary PVT compensation system. The PVT system comprises a reference block, a variation sensor block, a correction block and a driving stage. Of particularly noted, there are many possible circuit implementation alternatives for each block. The function for each block is described in the following.
Reference Block: The reference block is to provide the reference signal(s) such as $V_{\text{REF}}$ and $I_{\text{REF}}$. The voltage reference signal $V_{\text{REF}}$ can be used to define a precise $V_{\text{GS}}$ [44, 50] [46] or a precise body voltage [51] whereas the current reference signal $I_{\text{REF}}$ can be used to define the saturation current of the PMOS and NMOS transistors [45] in the digital logic gates. To generate $V_{\text{REF}}$ from the reference block, bandgap voltage references [52-58] are normally used because they can generate the precise output voltage with high temperature stability. CMOS voltage references [59-73] can also be used which can offer low voltage operation. But the CMOS voltage reference’s output voltage is dependent on process and the temperature stability is normally poorer than the BJT based counterparts. As for the reference current $I_{\text{REF}}$, it can be generated in different ways. First, a threshold monitoring circuit ($V_{\text{TH}}$ sensor) can be utilized. The $V_{\text{TH}}$ sensor can generate the extrapolated $V_{\text{TH}}$ of a single MOSFET absolute zero temperature ($V_{\text{TH0}}$) [61-63, 65]. In principle, $V_{\text{TH0}}$ is insensitive to variations in temperature and supply, but having a process-dependent characteristic. As such, after scaling the $V_{\text{TH0}}$ using resistors and applied the scaled $V_{\text{TH0}}$ to a saturated MOSFET, a PVT-invariant $I_{\text{REF}}$ can be generated [74]. Another way to generate $I_{\text{REF}}$ is to using V-I converter in [75]. By applying a proportional-to-absolute-temperature (PTAT) voltage to a resistor with positive T.C., a temperature invariant current can be achieved.

Fig. 1.6: Generic block diagram of an exemplary PVT compensation system.
However, due to the process variation of the resistor, the precision of $I_{\text{REF}}$ may degrade under modern technologies.

**Variation Sensor:** The $V_{\text{TH}}$ sensor can be used to sense the process variation [63] on the basis of the linkage between $V_{\text{TH0}}$ and delay. However, it cannot provide the temperature variation information. Another simple circuit is to use diode transistors to sense the process and temperature variation together [44, 45, 50]. Finally, a phase-lock-loop (PLL) can also be used to detect the parameter and timing error of the digital circuits under PVT variation but a precision high-frequency reference clock signal is required [76]. Besides, to relax the on-chip PLL filter size, the clock frequency tends to be very high as the design tradeoff.

**Correction Block:** To compensate the PVT variation, the correction techniques on the basis of substrate bias control to change the $V_{\text{TH}}$ of transistor are extensively reported [44-46, 48, 50, 51, 76-83]. At this juncture, it is common to observe that the effect of the substrate terminal on controlling the $V_{\text{TH}}$ of the transistor is significantly reduced due to relatively lower body bias factor in advanced nanometer CMOS process technologies. As a result, the substrate bias control to minimize the PVT variation [50] becomes less effective. In addition, the substrate leakage current is considered high under the process, thereby contributing the potential large power overhead. More importantly, reliability becomes another major concern when the operating temperature potentially reduces the gap of safety margin in a forward-biased substrate, hence increasing the risk of latch up. This imposes the difficulty of employing substrate bias control in nanometer VLSI systems. Another one is the post-silicon compensation technique that of adaptively changing the supply of digital circuits [78, 79]. This method is effective since the delay of the digital circuit is
heavily dependent on its supply voltage. However, the cost is increased because of the post-silicon trimming process.

**Driving Stage:** For the adaptive body bias correction technique, a voltage buffer is employed to distribute the body voltage [45]. For the adaptive supply compensation, the driving stage can be implemented in a form of DC-DC converter [45] or LDO regulators. Despite of the efficiency, the DC-DC converter has the key disadvantage of large switching noise. Of major design concern, it needs the off-chip capacitors and inductors that do not support the fully integration design objective. Therefore it may not be suitable for on-chip PVT compensation. In the context of the LDO regulators, the OCL-LDO regulator architecture with wide $C_L$ range driving capability becomes the optimum choice for use in driving the digital system.

From the above study of the PVT compensated system and the modern trend of low-power and variation-aware circuits in the advanced CMOS process technologies, they raise the motivation for the design of a total fully-integrated power management circuit/system with PVT supply compensation as the ultimate goal.
1.2 Objectives

Followed by the study and background work, the objectives of this thesis are:

(i) To investigate, design and implementation of a small T.C. $V_{TH}$ sensor.

(ii) To research new circuit technique and topology for the design of OCL-LDO regulators to drive wide range of $C_L$ with fast transient performance.

(iii) To exploit the design and implementation of a PVT compensation supply system for point-of-load digital circuits.

(iv) To conduct the detailed circuit analysis of the $V_{TH}$ sensor, the LDO regulators and the PVT compensation system.

(v) To conduct the test for the silicon prototypes which are realized in UMC 65-nm CMOS technology.
1.3 Contributions

The main contributions of this research work in this thesis are summarized as follows:

(i) Propose a nonlinear temperature compensation technique for the design of $V_{TH}$ sensor which can reduce the T.C. of the output voltage under low power constraint.

(ii) Propose a frequency compensation technique for the OCL-LDO regulator to extend the $C_L$ range. The regulator can achieve the widest $C_L$ range driving capability with good stability and transient performance.

(iii) Propose a current feedback technique for the OCL-LDO regulator which can drive a wide range of $C_L$ whilst achieving fast transient performance metrics with good regulation accuracy.

(iv) Propose a point-of-load digital system driving supply with PVT compensation. Such the PVT compensated supply (PVTCS) can reduce the performance deviation of digital circuits and demonstrate significant delay variation improvement with respect to that of the uncompensated digital supply counterpart.

Table 1.2 summarizes the proposed techniques together with their performances. It can be seen that all the proposed techniques have achieved good performance. As such, they are suitable for fully-integrated power management system with PVT compensation effects. First, the $V_{TH}$ sensor can be used to generate the process information or to generate a constant current. Second, the two wide $C_L$ range LDO regulators can be served as driver for digital load circuits. Lastly, using the circuit technique in Type-II LDO regulator, the PVTCS has demonstrated an exemplary fully on-chip power management system with PVT compensation.
### Table 1.2 Summary of Contributions in This Research Work

<table>
<thead>
<tr>
<th>Proposed Techniques</th>
<th>Performances and Technical Merits</th>
</tr>
</thead>
</table>
| $V_{TH}$ sensor     | 1. Low T.C. (24.5 ppm/°C)  
2. Wide Temperature Range (-40 °C to 90°C)  
3. Low power (290 nW)  
4. Operate well under nanometer technology |
| LDO Regulator (Type-I) | 1. Wide $C_L$ range (10 pF to 10 nF)  
2. Stable and work well from 0 to full loading current (50 mA).  
3. Simple structure  
4. Fast transient |
| LDO Regulator (Type-II) | 1. Wide $C_L$ range (470 pF to 10 nF).  
2. Small compensation capacitor (3.8pF).  
3. Stable and work well from 0 to full loading current (50 mA).  
4. Fast transient response with <400 ns settling time |
| PVTCS               | 1. Simple structure  
2. Can effectively compensate performance variations under PVT variations.  
3. Supply control with no latch up issue with respect to adaptive body bias. |
1.4 Organization of the Thesis

This report is organized in seven Chapters as follows.

Chapter 1 gives the motivations, objectives and contributions of this research.

Chapter 2 reviews the $V_{TH}$ sensor circuits pertaining to their temperature compensation principles. This is followed by the discussion and analysis of the proposed current-mode second-order temperature compensated $V_{TH}$ sensor.

Chapter 3 reviews the representative LDO regulator structures. The gain stage structure, stability, transient performances will be discussed. Layout techniques for regulators will also be described.

Chapter 4 presents the Type-I OCL-LDO regulator that can drive wide $C_L$ range. Detailed analysis is given. Simulation results are investigated and compared with the state-of-the-art OCL-LDO regulator topologies.

Chapter 5 presents the Type-II OCL-LDO regulator with wide $C_L$ range driving capability. Design strategies, stability analysis, simulation and measurement results are explored in detail.

Chapter 6 reviews the PVT compensation techniques. A PVT compensated supply to drive point-of-load digital system is introduced. The simulation and measurement results are discussed. The performance is compared with the benchmark work.

Chapter 7 gives the concluding remarks as well as the recommendations for the future works of this research.
CHAPTER 2

THRESHOLD MONITORING CIRCUIT

In this Chapter, a review of threshold monitoring ($V_{TH}$ sensor) circuit is first conducted. The temperature compensation principles for each design are discussed. This is followed by the proposed current-mode second-order temperature compensated $V_{TH}$ sensor. The operating principle, simulation and measurement results are discussed in detail.

2.1. Introduction

A voltage reference is commonly employed to generate a constant DC voltage for digital, analog as well as mixed-signal circuits and systems. The popular application examples are operational amplifiers, data converters, and power management circuits [1, 84]. Consider the bandgap voltage reference design using bipolar transistor (BJT), it can provide quite a precise voltage [52-58]. Unfortunately, due to the fixed 0.6 – 0.7 V PN junction turn-on voltage at room temperature, it requires a high supply voltage for operation headroom. Meanwhile, it does not give any hint in MOS process information thus cannot be applied as a process monitoring sensor. Turning to the voltage reference without BJTs counterparts [59-73], they offer low-voltage operation capability and linkage with process information. However, due to intrinsic transistor’s process parameters displaying relatively poor immunity against the process variations, there are few nanometer process based voltage reference designs [69-71] which achieve a small temperature coefficient (T.C.) under a wide temperature range.

Considering the $V_{TH}$ sensor circuit, it can generate the extrapolated $V_{TH}$ of a
MOSFET at absolute zero temperature ($V_{TH0}$) [61-63, 65]. $V_{TH0}$ is insensitive to the changes in temperature and supply, but it is process-dependent. With these characteristics, a $V_{TH}$ sensor can be used to sense the $V_{TH}$ of the MOSFET so as to provide the process information. It also can generate a PVT-invariant constant current source [74] or process dependent supply voltage for compensating the process variations in digital LSIs [45, 63]. However, the reported $V_{TH}$ sensor designs [61-63, 65] all use CMOS process technologies with large channel lengths. Therefore, if nanometer technology which is subject to large process variations is used, the difficulty to maintain their original low T.C. performance is increased.
2.2. Review of $V_{TH}$ Sensor Designs

This section discusses the reported $V_{TH}$ sensor designs. The temperature compensation principle, design challenges and considerations under nanometer technologies are all explored.

2.2.1. Ferreira’s $V_{TH}$ Sensor [62]

![Fig. 2.1: Ferreira’s $V_{TH}$ sensor circuit [62].](image)

Ferreira et al. proposes a $V_{TH}$ sensor circuit using linear resistor and weak inversion transistors [62] as shown in Fig. 2.1. It generates the PTAT voltage through injecting a PTAT current into a linear resistor ($R_2$) to compensate the negative T.C. of $V_{TH}$. $M_1$ and $M_3$ are implemented as a composite transistor as shown in enclosed area. It cascades two transistors in series to increase the output impedance, thus the accuracy of the PTAT generator is improved.

The output voltage of this design can be derived as follows:
\[ I_B(T) = \eta_p \frac{k_B T}{q R_t} \frac{1}{R_t} \ln \left( \frac{(W/L)_2}{(W/L)_4} \right) \]  

\( V_{GS4}(T) = V_{TH0} \left( 1 - \frac{T}{T_r} \right) + V_{GS4}(T_r) \left( \frac{T}{T_r} \right) + (1 - \alpha) \eta_n \frac{k_B T}{q} \ln \left( \frac{T}{T_r} \right) \)  \( 2.1 \)

\[ V_{OUT}(T) = \eta_p \frac{k_B T}{q R_t} R_2 \ln \left( \frac{(W/L)_2}{(W/L)_4} \right) + V_{GS4}(T) \]

\[ = V_{TH0} \left( 1 - \frac{T}{T_r} \right) + V_{GS4}(T_r) \left( \frac{T}{T_r} \right) + (1 - \alpha) \eta_n \frac{k_B T}{q} \ln \left( \frac{T}{T_r} \right) \]  \( 2.2 \)

\[ + \eta_p \frac{k_B T}{q R_t} R_2 \ln \left( \frac{(W/L)_2}{(W/L)_4} \right) \]

where \( \eta_p \) and \( \eta_n \) are the subthreshold slope factors for PMOS and NMOS respectively. \( \alpha \) is a process dependent parameter. After the minimum temperature dependence is achieved, the output voltage is

\[ V_{OUT}(T) = V_{TH0} - (1 - \alpha) \eta_n \frac{k_B T}{q} \left[ 1 - \ln \left( \frac{T}{T_r} \right) \right] \]  \( 2.3 \)

Referring to (2.4), the second term is small when compared with the first term. The output voltage is approximated as \( V_{TH0} \). This circuit is simple but the first order temperature compensation limits its T.C. performance.
2.2.2. Ueno’s V\textsubscript{TH} Sensor [63]

![Ueno's V\textsubscript{TH} sensor circuit][1]

**Fig. 2.2: Ueno’s V\textsubscript{TH} sensor circuit [63].**

Ueno et al. presents a V\textsubscript{TH} sensor circuit under 0.35-\textmu m process as shown in Fig. 2.2. It achieves 15 ppm/°C while consuming a power of 300 nW [63]. It compensates the negative T.C. of V\textsubscript{TH} through a stack of proportional-to-temperature (PTAT) voltage. Besides, the current generation is achieved by biasing a transistor (M\textsubscript{R}) at linear region using the output voltage.

In Fig. 2.2, the transistors M\textsubscript{1} to M\textsubscript{7} all work in subthreshold region while the transistor M\textsubscript{R} works in linear region. The output voltage of this circuit can be derived as follows:

\[
I_p = \frac{V_{\text{DSMR}}}{R_{MR}} = S_R \mu C_{\text{OX}} (V_{\text{OUT}} - V_{\text{TH}}) \eta V_T \ln \left( \frac{S_2}{S_1} \right) \tag{2.5}
\]

\[
I_0 = \mu C_{\text{OX}} (\eta-1)V_T^2 \tag{2.6}
\]
\[ V_{OUT} = V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \]
\[ = V_{GS4} + \eta V_T \ln \left( \frac{2S_3 S_5}{S_6 S_7} \right) \]
\[ = V_{Th} + \eta V_T \ln \left( \frac{3I_p}{S_4 I_0} \right) + \eta \ln \left( \frac{2S_3 S_5}{S_6 S_7} \right) \]
\[ = V_{TH0} - \kappa T + \eta \frac{k_B T}{q} \ln \left( \frac{3I_p}{S_4 I_0} \right) + \eta \frac{k_B T}{q} \ln \left( \frac{2S_3 S_5}{S_6 S_7} \right) \]

(2.7)

Substituting \( I_p \) into \( V_{OUT} \) and taking the derivative of \( V_{OUT} \) respect to \( T \), the final output voltage is \( V_{TH0} \) by setting the derivative to zero (the temperature dependent terms are cancelled). This means that the circuit yields the \( V_{TH0} \) after equalizing the negative and positive temperature dependent terms in ideal case.

The PTAT voltage inside this design is generated by stacking two transistors which are biased in saturated weak inversion region (\( M_3 \) & \( M_4 \), \( M_5 \) & \( M_6 \)). Under nanometer technology with a low threshold CMOS process, the \( V_{TH} \) of the NMOS transistor is small (< 400 mV at room temperature) when the channel length bigger than 500 nm. Moreover, to ensure that the transistor works in the saturated weak inversion region, \( V_{DS} \) must be bigger than 0.1 V [63]. This increases the design difficulty for the stacked transistors to work properly to generate a linear PTAT voltage. In addition, since the bias current \( I_p \) is generated through an active resistor, this T.C. may be sensitive to the process variation as far as the biasing voltage across the triode transistor \( M_R \) is minute.
2.2.3. Lee’s $V_{TH}$ Sensor [65]

![Diagram of Lee's $V_{TH}$ sensor circuit]

Lee et al. introduces a simple $V_{TH}$ sensor circuit using a saturation region diode as the output voltage generator. The current is also produced on the basis of a linear region active resistor as that in [63]. The circuit is shown in Fig. 2.3. The output voltage could be expressed by

$$I_R = \frac{V_{DSR}}{R_{MR}} = S_R \mu C_{OX} (V_{OUT} - V_{TH}) \eta V_T \ln \left( \frac{S_2}{S_1} \right)$$  \hspace{1cm} (2.8)

$$I_0 = \mu C_{OX} (\eta - 1) V_T^2$$  \hspace{1cm} (2.9)

$$V_{OUT} = V_{GS3}$$

$$= V_{TH0} - \kappa T + \frac{2NI_R}{S_3 \mu C_{OX}}$$  \hspace{1cm} (2.10)

$$= V_{TH0} - \kappa T + \sqrt{\frac{2NS_R (V_{OUT} - V_{TH0} + \kappa T) \eta V_T \ln \left( \frac{S_2}{S_1} \right)}{S_3}}$$
From (2.10), the output voltage could be derived as

\[ V_{OUT} = V_{TH0} - \kappa T + \frac{2N S \eta \ln \left( \frac{S_2}{S_1} \right) k_B T}{S_3 q} \]  

(2.11)

As a result, after the temperature dependent parts in (2.11) have been cancelled, the circuit gives an output voltage of \( V_{TH0} \). Owing to the simple structure, this \( V_{TH} \) sensor circuit has the ability to achieve a small T.C. However, since the positive T.C. current is generated through an active resistor, the performance is still sensitive to process variations as well.
2.3. Proposed V_{TH} Sensor [85]

A current-mode second-order temperature compensation technique is proposed to reduce the nonlinear temperature effect in the V_{GS} of MOSFET. It is achieved by utilizing the different temperature properties of the high resistive poly resistor and the P+ diffusion resistor. The nonlinear temperature effect of V_{GS}, circuit implementation, working principle of the second-order temperature compensation, results and discussions are presented as follows.

2.3.1. Nonlinear Temperature Effect of V_{GS}

When a MOS transistor operates in the weak inversion region, its V_{GS}(T) displays CTAT characteristic and a nonlinear temperature effect. This is due to the temperature dependency of carrier mobility (\(\mu(T)\)) and V_{TH}(T). When a MOSFET work in weak inversion region with its drain-to-source voltage V_{DS} > 0.1 V, the drain current can be approximated as

\[
I_D(T) \approx S\mu(T_r)\left(\frac{T}{T_r}\right)^{-m} C_{ox} (\eta-1)V_T^2 \exp\left(\frac{V_{GS}(T)-V_{TH}(T)}{\eta V_T}\right)
\]

(2.12)

By taking the ratio of I_D at T and T_r [I_D(T) and I_D(T_r)] based on (2.12), we have

\[
\frac{I_D(T)}{I_D(T_r)} = \left(\frac{T}{T_r}\right)^{2-m} \exp\left(\frac{q}{\eta k_B TT_r} \frac{A}{T}\right)
\]

(2.13)

where \(A = V_{GS}(T)T_r - V_{GS}(T_r)T + V_{TH}(T_r)T - V_{TH}(T)T_r\)

Since the transistor is biased by a PTAT current, I_D(T)/I_D(T_r) = T/T_r. In addition, V_{TH}(T) can be approximated as

\[
V_{TH}(T) = V_{TH}(T_r) - \theta(T - T_r) = V_{TH0} - \theta T
\]

(2.14)
where \( \theta \) is the T.C. of \( V_{TH} \) [63]. As such, \( V_{GS}(T) \) can be obtained as

\[
V_{GS}(T) = V_{TH0} + \left[ V_{GS}(T_r) - V_{TH0} \right] \frac{T}{T_r} + (m-1) \frac{\eta k_B T}{q} \ln \left( \frac{T}{T_r} \right) \tag{2.15}
\]

At the weak inversion region, since \( V_{GS}(T_r) < V_{TH0} \), the second term shows a CTAT characteristic. The third term contributes a nonlinear temperature effect because of the \( T \ln(T/T_r) \) term. Through a Taylor Series expansion, we can approximate \( T \ln(T/T_r) \) as

\[
T \ln \left( \frac{T}{T_r} \right) \approx T - T_r + (T - T_r)^2 / (2T_r) \tag{2.16}
\]

Substituting (2.16) into (2.15), \( V_{GS}(T) \) can be obtained as

\[
V_{GS}(T) = V_{TH0} - (m-1) \frac{\eta k_B T}{2q} \left[ V_{GS}(T_r) - V_{TH0} \right] \frac{T}{T_r} + (m-1) \frac{\eta k_B T^2}{2qT_r} \tag{2.17}
\]

Since \( m \) is usually between 1.5 to 2 for CMOS transistors [86], the second-order \( T^2 \) term is positive in (2.17). As a result, if a negative \( T^2 \) term is added to offset this nonlinear error, the objective of T.C. reduction can be achieved.

### 2.3.2. Circuit Implementation

To generate a negative \( T^2 \) term to offset the nonlinear temperature error in (2.17), the different temperature properties of Poly resistor and P+ diffusion resistor are used. The proposed \( V_{TH} \) sensor with current-mode second-order temperature compensation is shown in Fig. 2.4. It consists of a first-order Brokaw \( V_{TH} \) main circuit, a second-order temperature compensation current generator and an operational amplifier. The main circuit generates a current \( I_1 \) through a PTAT voltage source and a high resistive poly resistor (\( R_1 \)). The second-order temperature compensation current (\( I_2 \)) generator comprises a PTAT voltage source and a P+ diffusion resistor (\( R_3 \)). When \( I_1 \) is dumped...
into $R_2$ (high resistive poly), the temperature variability of $R_1$ and $R_2$ can cancel each other. A first-order PTAT voltage ($V_{I1} = V_{I1,1st} = 2I_1R_2$) is established. On the contrary, when $I_2$ is dumped into $R_2$, both first-order and second-order temperature compensation voltages ($V_{I2,1st}$, $V_{I2,2nd}$, respectively, $V_{I2} = V_{I2,1st} + V_{I2,2nd} = I_2R_2$) are generated because of the different temperature properties of $R_2$ and $R_5$. Finally, $V_R$ ($=V_{I1} + V_{I2} = V_{I1,1st} + V_{I2,1st} + V_{I2,2nd}$) can compensate for both the first-order and second-order term in $V_{GS_1}$ in (2.17).

Figure 2.5 shows the temperature compensation principle of $V_{TH}$ sensor in graphical illustration. As indicated, the T.C. difference between the poly resistor $R_2$ and the diffusion resistor $R_5$ yields a negative second-order compensation voltage term, which can compensate for the positive second-order term of $V_{GS}$ in (2.17).

To ensure that an identical current flows through $R_3$ and $R_4$ ($R_3 = R_4$), as well as $M_1$ and $M_2$, an operational amplifier is utilized to equalize the voltages $V_A$ and $V_B$. The capacitor $C_1$ is used to increase power supply rejection (PSR) at high frequencies. The capacitor $C_2$ is added to maintain the stability of the loop. The working principle of the
$V_{TH}$ sensor and the second-order temperature compensation effect are explained as follows.

2.3.3. Working Principle

If $M_1$ and $M_2$ work in the weak inversion region, and assuming that $V_{TH1}(T) = V_{TH2}(T)$, $I_{DS1}(T) = I_{DS2}(T) = I_1$, we have $\Delta V_{GS} = V_{GS1} - V_{GS2} = \eta V_T \ln(S_2/S_1)$ according to (2.12). Hence, the currents $I_1$ and $I_2$ can be expressed in the form as $I_1 = \left[\eta V_T \ln\left(S_2/S_1\right)\right]/R_1(T)$ and $I_2 = \left[N\eta V_T \ln\left(S_3/S_4\right)\right]/R_5(T)$, respectively. $N (= S_9/S_8)$ is the current mirror ratio for $M_9$ to $M_8$ in Fig. 2.4. The output voltage is obtained as

$$V_{OUT} = V_R + V_{GS1}(T) = 2I_1R_2(T) + I_2R_2(T) + V_{GS1}(T)$$

$$= 2\eta \frac{k_BT}{q} R_2(T) \ln\left(\frac{S_2}{S_1}\right) + N\eta \frac{k_BT}{q} R_5(T) \ln\left(\frac{S_4}{S_3}\right) + V_{GS1}(T)$$

(2.18)

where $V_{GS1}(T)$ is defined by (2.17). From (2.18), since $R_1$ and $R_2$ are both poly resistor and they have a similar T.C., $R_2(T)/R_1(T) \approx R_2(T_i)/R_1(T_i)$. In addition, based on a first-

Fig. 2.5: Temperature compensation in graphical illustration.
order temperature modeling of $R_2(T)$ and $R_5(T)$, $TR_2(T)/R_5(T)$ in the second term of (2.18) can be approximated as

$$\frac{T \cdot R_2(T)}{R_5(T)} = \frac{R_2(T)}{R_5(T)} \left[ 1 + \alpha(T - T_r) \right]$$

$$\approx \frac{R_2(T)}{R_5(T)} \left[ 2(\alpha - \beta)T_r + 1 \right] + (\alpha - \beta)T^2 + (\alpha - \beta)T_r^2 \right\}$$

using a Taylor Series expansion. In (2.19), $\alpha$ is the T.C. of $R_2(T)$ and $\beta$ is the T.C. of $R_5(T)$. Since $\alpha < 0$, and $\beta > 0$, the $T^2$ term is negative. It can be used to offset the positive $T^2$ term in $V_{GS1}(T)$ in (2.17). Substituting (2.19) in (2.18), $V_{OUT}$ can be obtained as

$$V_{OUT} = V_{GS1}(T) + 2\eta \frac{k_BT}{q} R_2(T_r) \ln \left( \frac{S_2}{S_1} \right) + N\eta \frac{k_BT}{q} R_5(T_r) \ln \left( \frac{S_4}{S_5} \right)$$

$$\times \left[ 2(\alpha - \beta)T_r + 1 \right] + (\alpha - \beta)T^2 + (\alpha - \beta)T_r^2 \right\}$$

$$\approx V_{TH0}$$

From (2.20), by choosing the appropriate values for $R_1$, $R_2$ and $R_5$, $V_{OUT}$ can be optimized to obtain a zero T.C., with its final value being approximately equal to $V_{TH0}$.

Figure 2.6(a) depicts the simulated $V_{GS1}$ and $V_{I2}$ ($V_{I2} = I_2R_2$) and their slopes with respect to temperature. When the temperature increases, $V_{GS1}$ decreases but the falling rate is continually reduced. This correlates with the analytical result in Section 2.3.1 that the $T^2$ term in $V_{GS1}(T)$ is positive. The second-order compensation voltage $V_{I2}$ has a PTAT characteristic, with its positive slope decreasing as well. This confirms that the $T^2$ term in $V_{I2}$ is negative. To compare the T.C. performance of $V_{TH}$ sensors with and without the second-order compensation, a first-order Brokaw $V_{TH}$ sensor is built and simulated. It is constructed by removing the second-order current generator in Fig. 2.4.

In addition, resistor $R_2$ is increased to achieve optimal temperature compensation. To evaluate the performance of the circuit under process variations, Monte-Carlo (MC)
simulations are conducted. Transistor parameters including threshold voltage, mobility, and subthreshold slope factor are simulated across random process variations [71]. All the MC simulations in this Chapter are carried out with a sample size of 500 and 3 standard deviation (3σ) coverage. Figure 2.6(b) depicts the MC simulation results of T.C. for the first-order Brokaw circuit and the proposed VTH sensor. The results suggest that the second-order temperature compensation reduces the mean T.C. of the VTH sensor by 40%. It is noted that the standard deviation increases slightly with 1.8 ppm/°C. This fact stems from different variations for poly and diffusion resistors. However, the total first-order T.C. variation (Mean + Stdv.) of 81.7 ppm/°C (first-order) is reduced to the T.C. of 53.5 ppm/°C with first-order plus second-order compensation. This has confirmed that the second-order temperature compensation technique can reduce the nonlinear temperature effect of MOSFET VGS and improve the temperature stability of a VTH sensor.

![Fig. 2.6: (a) Simulated VGS1, V12 and their slopes with respect to temperature variation. (b) Monte-Carlo simulation results for first-order Brokaw circuit and proposed temperature compensated VTH sensor.](image)

Figure 2.7 shows the simulated VOUT under different temperature and supply voltages. It can be seen that the VTH sensor can generate a stable output voltage when both temperature and supply varies. Figure 2.8 depicts the Monte-Carlos simulation
result for PSR @ 100 Hz. The mean PSR value is -38dB and the worst case PSR is still smaller than -30 dB.

**Fig. 2.7** Simulated $V_{OUT}$ under different supply voltages and temperatures.

**Fig. 2.8** Monte-Carlo simulation results for PSR @ 100 Hz.
2.3.4. Results and Discussions

The proposed $V_{TH}$ sensor is implemented in a UMC 65-nm CMOS process. The microphotograph is shown in Fig. 2.9. It occupies an active area of 0.0198 mm$^2$.

![Microphotograph of the proposed $V_{TH}$ sensor.](image)

**Fig. 2.9: Microphotograph of the proposed $V_{TH}$ sensor.**

2.3.4.1. Measurement Setup and Calibration Procedure

To tackle the leakage effect of the I/O pads, a voltage buffer (non-inverting unity-gain Op-Amp) is added at the output of the $V_{TH}$ sensor. The T.C. of the voltage buffer is also measured and subtracted from the measured output T.C. to get the actual T.C. performance of $V_{TH}$ sensor.

Since $R_1$, $R_2$ and $R_5$ may deviate from the design values due to process variations, a 4-bit binary weighted calibration is implemented for resistor $R_2$. The calibration scheme is based on 2 temperature measurements. A successive approximation method is used in the process without exceeding maximum of 4 calibration steps. First, the voltage at the maximum temperature (90 °C, $V_{TMAX}$) and the minimum temperature (-40 °C, $V_{TMIN}$) are measured. Second, if $V_{TMAX}$ is bigger than $V_{TMIN}$, this indicates that PTAT voltage is too strong. $R_2$ is then reduced. If $V_{TMAX}$ is smaller than $V_{TMIN}$, this
indicates that PTAT voltage is too weak. R₂ is then increased. The calibration is conducted iteratively and stopped when \( V_{\text{TMAX}} = V_{\text{TMIN}} \) [57].

2.3.4.2. Measurement Results

The \( V_{\text{TH}} \) sensor can operate from a supply of 0.75 V to 1.2 V with a temperature range of -40 °C to 90 °C. The power consumption measured at room temperature is 290 nW at a supply of 0.75 V. In this study, 15 samples were measured. Figure 2.10(a) depicts the measured \( V_{\text{OUT}} \) as a function of temperature at a 0.75 V supply, and shows that \( V_{\text{OUT}} \) is very stable across temperature variation for each sample. Figure 2.10(b) shows the DC output voltage against temperature at different supply voltages. Compared with the simulated results in Fig. 2.7, \( V_{\text{OUT}} \) becomes smaller due to the process variation. However, a stable \( V_{\text{OUT}} \) can still be achieved. This validates that the \( V_{\text{TH}} \) sensor can work well from 0.75 V to 1.2 V.

![Fig. 2.10](image) (a) Measured output voltage \( V_{\text{OUT}} \) as a function of temperature for 15 samples with 0.75V supply voltage. (b) Measured output voltage \( V_{\text{OUT}} \) as a function of temperature for different supply voltages.

Figure 2.11(a) shows the distribution of \( V_{\text{OUT}} \) at room temperature. The measured mean output voltage (\( V_{\text{OUT,MEAN}} \)) is 474 mV with a standard deviation of 16 mV. Figure 2.11(b) depicts the measured T.C. distribution. Due to the proposed second-order compensation technique, the \( V_{\text{TH}} \) sensor achieves a minimum T.C. of 24 ppm/°C.
and a maximum T.C. of 50.4 ppm/°C. The average T.C. is 40 ppm/°C with a standard deviation of 8.5 ppm/°C.

Figure 2.11: (a) Distribution of $V_{OUT}$ for 15 samples at room temperature. (b) Distribution of the T.C. performance metric for 15 samples.

Figure 2.12(a) illustrates the measured power supply rejection (PSR) for the $V_{TH}$ sensor, which is -40 dB at 100 Hz and it’s closed to the simulation results in Fig. 2.8. Figure 2.12(b) depicts the supply ripple response. When a sine wave ($f = 100$ Hz, amplitude = 100 mV$_{pp}$) is applied at the supply, the measured output ripple is about 1.04 mV$_{pp}$.

Figure 2.12: (a) Measured PSR. (b) Measured power supply ripple response at $V_{DD} = 0.75$ V, $V_{ripple} = 100$ mV for the proposed $V_{TH}$ sensor.
2.3.4.3. Scalability and Process Variations

Due to the precision analog design and the use of nonlinear terms and second-order effects, scaling cannot be directly applied. But the usual design steps for the $V_{TH}$ sensor remain the same. Under different process technologies, based on (2.17) and (2.20), the ratio of $R_1/R_2$ and $R_5/R_2$ can be optimized to achieve first and second-order compensation, respectively. First, for the first-order compensation, $R_1$ and $R_2$ should be of the same type. Second, for a $V_{GS}$ to have a positive nonlinear second-order term, the T.C. for $R_5$ must be positive whereas the T.C. for $R_2$ must be negative. On the contrary, for a $V_{GS}$ to have a negative nonlinear second-order term, the T.C. for $R_5$ must be negative while the T.C. for $R_2$ must be positive. This fact will enable a low T.C. $V_{TH}$ sensor to be designed with different technologies.

Process variations are discussed in two parts: (i) Die-to-Die (D2D) variations and (ii) Within-Die (WID) variations.

(i) Die-to-Die variations: All devices on the same die are assumed to be affected in the same way [50]. Since temperature compensation depends on resistor ratios, based on (2.20), the first-order compensation leads to approximately no change. In addition, the use of different resistor types for $R_2$ and $R_5$ mean that the variation in the $R_2/R_5$ ratio will lead to some deviation in the T.C. However, MC simulation results show that this T.C. drift is still low in the proposed $V_{TH}$ sensor (Fig. 2.13(a)). Under D2D variations, the T.C. shows a 5.6 ppm/°C standard deviation.

(ii) Within-Die variations: In this scenario, devices on the same die are assumed to behave differently [50]. This local device mismatch also affects the behavior of the output. However, the MC simulation results (Fig. 2.13(b)) (T.C. standard deviation = 4.3 ppm/°C) illustrate that the $V_{TH}$ sensor has a small sensitivity to WID variations.
To explain the effect using examples, the $V_{TH}$ mismatch of $M_1$ and $M_2$, $R_3$ and $R_4$ in Fig. 2.4 are then discussed next. If it is assumed that $V_{TH1} = V_{TH2} + \Delta V_{TH}$, where $\Delta V_{TH}$ is the mismatch error, based on (2.12), the generated non-ideal PTAT voltage ($\Delta V_{GS,n}$) across $R_1$ can be obtained as

$$\Delta V_{GS,n} = V_{GS1} - V_{GS2} - (V_{TH1} - V_{TH2}) = \eta V_T \ln(S_2/S_1) + \Delta V_{TH}$$  \hspace{1cm} (2.21)

If $\Delta V_{TH}$ is constant, an offset voltage ($V_{offset}=\Delta V_{TH}R_2/R_1$) will contribute to the $V_{TH0}$. Figure 2.14 (a) depicts $V_{OUT}$ under MOSFET-devices-only WID variations. It shows that the standard deviation is only 4.6 mV. This is smaller than 1% of the mean value. In addition, even with an offset error, $V_{OUT}$ can still link with process information so as to provide a threshold monitoring function.

In terms of the mismatch of $R_3$ and $R_4$, if it is assumed that $R_3/R_4=(1+\sigma)$, $V_A=V_B$ and $V_{TH1}=V_{TH2}$, where $\sigma$ is the mismatch error (in ratio) between $R_3$ and $R_4$, a non-ideal PTAT voltage is generated as follows:

$$\Delta V_{GS,n} = V_{GS1} - V_{GS2} = \eta V_T \ln(S_2/[(1+\sigma)S_1])$$  \hspace{1cm} (2.22)
From (2.22), the mismatch error of $R_3$ and $R_4$ modifies the slope of PTAT voltage, which subsequently changes the level of temperature compensation. Figure 2.14(b) depicts the T.C. under resistors-only WID variations, confirming that the T.C. is stable with typical variation.

**Fig. 2.14:** (a) Monte-Carlo simulation results of $V_{OUT}$ for MOSFET-devices-only within-die variations. (b) Monte-Carlo simulation results of T.C. for resistors-only within-die variations.

### 2.3.4.4. Performance Comparison

The performance comparisons of the proposed $V_{TH}$ sensor with the reported nanometer voltage reference circuits and $V_{TH}$ sensors are depicted in Tables 2.1 and 2.2, respectively. Refer to Table 2.1, the voltage references [69, 70] display relatively larger T.C. values and significantly larger power. Despite another design [71] consumes smaller power and area, but it does not provide the process information based on the voltage generation method. Besides, the minimum T.C. is around 4 times and the maximum T.C. is more than 2 times with respect to this work. It turns out that this work offers good balanced performance metrics in nanometer voltage reference design. Refer to Table 2.2, the T.C. of the proposed $V_{TH}$ sensor is close to that of the reported counterparts [61-63, 65] in large channel-length technologies. Table 2.3
presents the performance comparison of the proposed $V_{TH}$ sensor with the BJT based bandgap voltage reference. It can be seen that the proposed $V_{TH}$ sensor consumes the smallest power whilst achieve a comparable T.C. performance with respect to the BJT bandgap voltage reference. Most importantly, the proposed $V_{TH}$ sensor can generate the $V_{TH}$ of the transistor at 0 K and provide the process information. In summary, the proposed threshold monitoring circuit can provide good temperature stability, wide temperature range, low supply operation and relax the design difficulty to obtain lower T.C. in the context of design challenges in nanometer CMOS technology.

| TABLE 2.1 PERFORMANCE COMPARISON OF THE PROPOSED $V_{TH}$ SENSOR WITH OTHER REPORTED NANOMETER CMOS VOLTAGE REFERENCE CIRCUITS |
|---|---|---|---|---|---|
| | [69] | [69] | [70] | [71] | This Work |
| Year | 2008 | 2008 | 2009 | 2012 | 2014 |
| Technology (nm) | 90 | 90 | 32 | 65 | 65 |
| Temp. Range (°C) | 10-100 | 5-100 | 0-125 | -20-80 | -40-90 |
| $V_{DD}$ (V) | 0.55-1 | 0.55-1 | 0.9-1.4 | 0.5-2.5 | 0.75-1.2 |
| $V_{OUT}$ (mV) | 251 | 243 | 540 | 330.1 | 474 |
| Power (nW) | 375000 | 547000 | 12600 | 0.24 | 290 |
| Min. T.C. (ppm/°C) | 263 | 160 | 962 | 89.1 | 24 |
| Max. T.C. (ppm/°C) | N/A | N/A | N/A | 118.2 | 50.4 |
| Mean T.C. (ppm/°C) | N/A | N/A | N/A | N/A | 40 |
| Line Sens. (ppm/V) | 119522 | 123457 | N/A | 3300 | 2423 |
| PSR (dB) (@100 Hz) | N/A | N/A | N/A | -40 | -40 |
| Chip Area (mm$^2$) | 0.019 | 0.07 | 0.016 | 0.0009 | 0.0198 |
| No. of Samples | 18 | 16 | N/A | 17 | 15 |
### TABLE 2.2 PERFORMANCE COMPARISON OF THE PROPOSED NANOMETER \( V_{\text{TH}} \) SENSOR WITH OTHER REPORTED \( V_{\text{TH}} \) SENSOR DESIGNS USING LONG CHANNEL-LENGTH TRANSISTORS

<table>
<thead>
<tr>
<th>Year</th>
<th>[61]</th>
<th>[62]</th>
<th>[63]</th>
<th>[65]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (µm)</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
<td>0.13</td>
<td>0.065</td>
</tr>
<tr>
<td>Temp. Range (°C)</td>
<td>0-80</td>
<td>-20-80</td>
<td>-20-80</td>
<td>-50-130</td>
<td>-40-90</td>
</tr>
<tr>
<td>( V_{DD} ) (V)</td>
<td>0.9-4</td>
<td>0.95-3</td>
<td>1.4-3</td>
<td>0.7-1.8</td>
<td>0.75-1.2</td>
</tr>
<tr>
<td>( V_{OUT} ) (mV)</td>
<td>670</td>
<td>741</td>
<td>745</td>
<td>501</td>
<td>474</td>
</tr>
<tr>
<td>Power (nW)</td>
<td>36</td>
<td>390 (@80°C)</td>
<td>300</td>
<td>210</td>
<td>290</td>
</tr>
<tr>
<td>Min. T.C. (ppm/°C)</td>
<td>10</td>
<td>38.8</td>
<td>7</td>
<td>23.8</td>
<td>24</td>
</tr>
<tr>
<td>Max. T.C. (ppm/°C)</td>
<td>N/A</td>
<td>40.1</td>
<td>45</td>
<td>41.1</td>
<td>50.4</td>
</tr>
<tr>
<td>Mean T.C. (ppm/°C)</td>
<td>N/A</td>
<td>39</td>
<td>15</td>
<td>29.3</td>
<td>40</td>
</tr>
<tr>
<td>Line Sens. (ppm/V)</td>
<td>2700</td>
<td>32524</td>
<td>20</td>
<td>337</td>
<td>2423</td>
</tr>
<tr>
<td>PSR (dB) (@100 Hz)</td>
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<td>-23.4 (@1kHz)</td>
<td>-45</td>
<td>N/A</td>
<td>-40</td>
</tr>
<tr>
<td>Chip Area (mm²)</td>
<td>0.045</td>
<td>0.0759</td>
<td>0.055</td>
<td>0.023</td>
<td>0.0198</td>
</tr>
<tr>
<td>No. of Samples</td>
<td>20</td>
<td>3</td>
<td>17</td>
<td>12</td>
<td>15</td>
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</table>

### TABLE 2.3 PERFORMANCE COMPARISON OF THE PROPOSED NANOMETER \( V_{\text{TH}} \) SENSOR WITH BANDGAP VOLTAGE REFERENCE CIRCUITS

<table>
<thead>
<tr>
<th>Year</th>
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<th>[57]</th>
<th>[58]</th>
<th>This Work</th>
</tr>
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<tbody>
<tr>
<td>Technology (µm)</td>
<td>0.4</td>
<td>0.6</td>
<td>0.6</td>
<td>0.35</td>
<td>0.16</td>
<td>0.065</td>
</tr>
<tr>
<td>Temp. Range (°C)</td>
<td>27-125</td>
<td>0-100</td>
<td>0-100</td>
<td>-20-100</td>
<td>-40-125</td>
<td>-40-90</td>
</tr>
<tr>
<td>( V_{DD} ) (V)</td>
<td>2.2-4</td>
<td>0.98</td>
<td>2-4</td>
<td>1.4</td>
<td>1.8</td>
<td>0.75-1.2</td>
</tr>
<tr>
<td>( V_{OUT} ) (mV)</td>
<td>518</td>
<td>603</td>
<td>1142</td>
<td>858</td>
<td>1087.5</td>
<td>474</td>
</tr>
<tr>
<td>Power (µW)</td>
<td>4.62</td>
<td>17.64</td>
<td>46</td>
<td>162</td>
<td>99</td>
<td>0.29</td>
</tr>
<tr>
<td>Min. T.C. (ppm/°C)</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>5</td>
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<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
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<td>Mean T.C. (ppm/°C)</td>
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<td>15</td>
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<td>12.4</td>
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<td>40</td>
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<td>Line Sens. (ppm/V)</td>
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<td>N/A</td>
<td>N/A</td>
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<td>0.057</td>
<td>1.152</td>
<td>0.12</td>
<td>0.0198</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
<td>61</td>
<td>15</td>
</tr>
</tbody>
</table>
2.4. Summary

In this Chapter, three $V_{TH}$ sensor designs are reviewed. The temperature compensation principles and the design difficulties under nano-meter technology are discussed. In the proposed $V_{TH}$ sensor topology, by using the different temperature properties of P+ diffusion and poly resistors, a current-mode based second-order temperature compensation effect is achieved. The simulation and measurement results have demonstrated that it has achieved better T.C. performance metrics than those of reported nanometer technology based voltage references. At the same time, its performance is also comparable with other reported $V_{TH}$ sensor circuits using long channel-length CMOS technologies. Therefore, the proposed $V_{TH}$ sensor is useful for on-chip sensing applications that require good temperature stability.
CHAPTER 3

REVIEW OF LDO REGULATORS

In this Chapter, the conventional output capacitor based LDO (OC-LDO) regulator topology is firstly discussed. This is followed by the review of output capacitorless (OCL-LDO) regulators based on different gain stage topologies. The stability and transient responses of the capacitor and capacitorless LDO regulators will be explored. Advantages and limitations of each topology are also presented. Finally, the layout techniques for LDO regulator are also described.

3.1. Conventional Output Capacitor LDO (OC-LDO) Regulator Structure

![Fig. 3.1: Conventional buffer based LDO regulator.](image-url)
The conventional buffer based OC-LDO regulator is shown in Fig. 3.1. It consists of an error amplifier, a buffer stage, a power transistor, a resistor feedback network and a voltage reference. The feedback signal is compared with the stable voltage reference ($V_{REF}$), thus generating a control signal at the gate of power transistor ($M_p$) to give a regulated output voltage of $(1+R_1/R_2)V_{REF}$. Due to the large size of $M_p$, there is a large parasitic capacitance ($C_P$) associated with the gate of power MOS which limits the response of the regulator.

This LDO regulator structure is intrinsically unstable because of the existence of three low-frequency poles ($p_1$, $p_2$ and $p_3$) in the feedback loop. They are located at the output node, at the output of error amplifier and the gate of $M_p$. In usual practice, a zero is created using an off-chip capacitor ($C_{out}$) through its ESR (equivalent series resistance) which aims to cancel the pole at the output of error amplifier. Figure 3.2 shows the loop gain response of the conventional LDO regulator. With the addition of a low-impedance voltage buffer, the large parasitic capacitance $C_P$ is tackled for the high output impedance of error amplifier. This pushes this parasitic pole to high frequency to stabilize the LDO regulator.

**Fig. 3.2: Loop gain response for conventional buffer based LDO regulator.**
The disadvantage of source follower implementation is that its voltage swing is restricted, especially under low supply voltage condition. Low output swing of buffer demands a large power transistor size, resulting in large parasitic capacitance as well as larger quiescent current to push \( p_3 \) to high frequency.

Refer to the transient responses of the conventional LDO regulator during load current (\( I_L \)) switching whilst prior to the feedback loop response, the output capacitor can function as a battery to source/sink current. Therefore, this permits a small undershoot/overshoot effect at the output voltage. The transient response time [1] can be expressed as

\[
t_r = \frac{1}{BW_{CL}} + C_P \frac{\Delta V}{I_{sr}}
\]

(3.1)

where \( BW_{CL} \) is the closed-loop bandwidth of the system, \( C_P \) is the parasitic capacitance at the gate of power transistor, \( \Delta V \) is the voltage change associated with the \( C_P \) and \( I_{sr} \) is the slew rate limited current. For fast transient response, a large closed-loop bandwidth and slew rate are needed. If the loop bandwidth is extended, \( p_3 \) may locate inside the unity gain frequency (\( \omega_{UGF} \)) which greatly limits the stability of LDO regulator. This is resolved at the expense of increasing quiescent power in the buffer stage so as to push \( p_3 \) beyond \( \omega_{UGF} \). Besides, fast transient implies high slew rate performance metric which is also translated to the large power consumption. These two factors contribute to the design tradeoff for power consumption.
3.2. Dynamic Biasing and Current Boosting in LDO Regulators

To overcome the potential large quiescent current problem in the topology depicted in Fig. 3.1, the dynamic biasing technique is implemented in the buffer stage design [11]. As illustrated in Fig. 3.3, it injects a $I_L$ dependent biasing current into the buffer stage to enable the parasitic pole $p_3$ to be shifted to high frequency. When $I_L$ increases, the buffer impedance is also simultaneously reduced so that it gives another aid for pushing the parasitic pole to higher frequency. This guarantees the stability of LDO regulator at all $I_L$ conditions. Using the same concept in [87], an error amplifier with dynamic biasing with respect to $I_L$ change is utilized. This improves the transient metrics whilst without sacrificing the quiescent power consumption.

During transient condition, a large current will flow to charge or discharge the parasitic capacitance $C_P$ of power transistor. Such the large transient current only appears in the transient state instead of the steady state. A current boosting technique [6] is reported. It momentarily injects a current into the buffer stage enhance the transient performance of the LDO regulator. This provides a low-quiescent fast-transient solution.

![Fig. 3.3: Dynamic biased LDO regulator.](image-url)
3.3. Output Capacitorless LDO (OCL-LDO) Regulator

The conventional OC-LDO regulators usually rely on a large off-chip capacitor to form part of the frequency compensation in the design. From fully integration viewpoint, it may not be favorable for on-chip applications. This increases the popularity of OCL-LDO regulators. Based on the gain stage structures, a review of OCL-LDO regulators including the stability and transient performance is conducted in this section.

3.3.1. Single-Stage Error Amplifier Plus Power Transistor OCL-LDO Regulator Topology

The topology in Fig. 3.4 shows the single-stage error amplifier plus the power transistor OCL-LDO regulator. The capacitor $C_L$ represents the parasitic capacitance of the loading circuit. For the stability of the regulator, there are two poles inside unity gain frequency $\omega_{UGF}$. If the transistor size of $M_P$ is large, the parasitic capacitance $C_{gd}$ of $M_P$ becomes big such that it can serve as Miller compensation capacitor. The pole-splitting process generates a dominant low-frequency pole $p_1$ at the output of error

\[ \text{Fig. 3.4: Single-stage error amplifier plus power transistor OCL-LDO regulator topology.} \]
amplifier. At low $I_L$, the impedance at the output node is not low enough, causing a low-frequency pole $p_2$ associated with $C_L$. The loop gain frequency response of conventional OCL-LDO regulator at low $I_L$ is presented in Fig. 3.5. To further stabilize the regulator, a Miller compensation capacitor can be added across the power transistor to ensure the location of $p_1$ at a sufficient lower frequency whilst $p_2$ at a sufficient higher frequency.

![Pole from output of Error Amp.](image)

**Fig. 3.5: Loop gain frequency response of the single-stage error amplifier plus power transistor OCL-LDO regulator at low $I_L$.**

In order to drive the potential large size power transistor in the generic LDO architecture of Fig. 3.4, many well-known circuit techniques have been reported to increase the speed of the error amplifier [28, 31, 88, 89]. In [88], the topology is a push-pull output amplifier which relaxes the tradeoff between the small quiescent current and slew rate (SR) at the gate of power transistor. It is further improved in [28] in which a current subtractor is utilized to extend the attainable gain bandwidth (GBW). In [89], a class-AB amplifier together with an assistant push-pull output stage circuit is employed to improve the transient response. Since the transconductance ($g_m$)
of amplifier is intentionally made small to achieve stability, the GBW of regulator is small. This results in a large settling time. In [31], a class-AB transconductance amplifier (OTA) having large output current capability and output resistance is adopted. With the aid of a flipped voltage follower (FVF) based tail current booster and a direct voltage spike detection SR enhancement circuit, the regulator can settle fast with improved transient responses.

In modern CMOS technology, the output impedance of transistor becomes relatively smaller than that of long-channel counterpart. This often yields a small loop gain factor in the feedback loop of Fig. 3.4. The price paid for that will be translated to the poor regulation accuracy.

3.3.2. Multi-Stage Error Amplifier Plus Power Transistor Regulator Topology

To guarantee good regulation accuracy, the loop gain of the regulator should be high. Therefore, the error amplifier in Fig. 3.4 will be realized in a form of multi-gain stage (2 stages or more) topology. Figure 3.6 illustrates a generic OCL-LDO regulator architecture featuring a multi-gain stage based error amplifier with a power transistor output stage.

![Fig. 3.6: Multi-gain stage error amplifier plus power transistor OCL-LDO regulator topology.](image)

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In Fig. 3.6, $g_{mi}$ denotes the transconductance while $R_i$ and $C_i$ are the equivalent output resistance and lumped output parasitic capacitance of the i-th gain stage, respectively. $R_O$ is the effective output resistance which includes the output resistance of power transistor as well as the loading resistance $R_L$. As indicated, the feedback system displays a four-pole ($p_{3dB}$, $p_2$, $p_3$ and $p_O$) characteristic. In general design, $p_O$ locates at a lower frequency than that of $p_2$ and $p_3$. Hence, $p_2$ and $p_3$ must be allocated to a high frequency to ensure the stability. The typical implementation of 2nd and 3rd gain stages is to keep node $N_2$ as a low impedance node ($R_2 \approx 1/g_{in}$) whereas node $N_P$ as a high impedance node [20, 24, 25, 27, 30]. Since $C_P$ is large on the basis of a large power transistor $M_P$, $p_3$ is low especially under low power constraint. As reported in [24], two parasitic poles are generated with frequency inversely proportional to $C_L R_O$. To stabilize the LDO regulator, $C_L$ must be small. Moreover, since $R_O$ is inversely proportional to $I_L$, a minimum $I_L$ (e.g. 3 mA) is required to ensure a small $R_O$ [24]. This restricts the application of this topology for wide $C_L$ and $I_L$ range application.

Turning to the transient speed of the LDO regulator architecture in Fig. 3.6, owing to the fixed bias and high output impedance characteristics in the 3rd gain stage, the speed at gate of power transistor becomes slow. This leads to large overshoot/undershoot as well as large settling time for the output voltage during $I_L$ switching. Meanwhile, the fixed bias in 1st stage error amplifier limits the unity gain frequency of the feedback loop. This restricts the speed of the LDO regulator. To tackle this issue, the adaptively bias technique [13, 25, 27, 30] can be realized to increase the biasing current of 1st stage error amplifier when $I_L$ increases. Unfortunately, it is hard to control for regulator’s stability because of positive feedback involved in the adaptively bias circuit.
3.3.3. Flipped-Voltage-Follower (FVF) Based OCL-LDO Regulator Topology

![Diagram](image)

**Fig. 3.7:** OCL-LDO regulator with Flipped Voltage Follower (FVF).

To reduce the impedance of the output node, a FVF based LDO regulator is proposed [22] as shown in Fig. 3.7. The output voltage is the reference voltage plus the $V_{GS}$ of $M_1$. The impedance of the output node at low $I_L$ becomes $1/g_{m1}$ which is considered to be small. During transient transition, $M_1$ senses the output voltage changes and serves as a common gate amplifier. It amplifies the signal and couples it to the gate of power transistor. The FVF structure does not need any compensation capacitor to stabilize the LDO regulator as proved in [22]. Unfortunately, a large power transistor size is often required to reduce the swing of gate voltage to avoid jeopardizing the operation region of $M_2$ and current source transistor. This introduces large parasitic capacitance at the gate of $M_p$. As a result, the speed of the regulator is limited under low power constraint. To address the limited bias current in the FVF topology in Fig. 3.7, a voltage spike detection circuit is added [23] to increase the biasing current momentarily during load current switching. Hence, the biasing current
during transient event is significantly increased. This momentarily current can effectively increase the speed of regulator without consuming large quiescent current. Since both circuits [22, 23] suffer from limited loop gain, they display poor load regulation, line regulation and PSR performance. In [24], an extra gain stage is inserted to increase the loop gain of the conventional FVF LDO regulator. This yields the additional high impedance node. This turns out that the stability is sacrificed at low $I_L$.

For a $C_L$ of 50 pF, the minimum $I_L$ is 1.5 mA at $V_{DD} = 0.75$ V and 3 mA at $V_{DD} = 1.2$ V. When $C_L$ increases, the corresponding increase of minimum $I_L$ is not favored in the low-quiescent LDO regulator design.

In summary, the OCL-LDO regulator eliminates the off-chip capacitor to achieve voltage regulation and hence can be fully integrated with the loading circuit and reduce the cost. However, without the output capacitor to form the dominant pole and source/sink current during load current switching, the loop stability and fast transient response are still the main design challenges for the OCL-LDO regulators, especially under low voltage, low quiescent current and wide $C_L$ range conditions.
3.4. Layout Techniques

To accomplish high-performance analog circuit, a proper layout is essential. This is because the device properties including matching, parasitic capacitances, parasitic resistance, noise and so forth are all dependent on the critical circuit layout. Turning to the layout aspect of LDO regulator, the layout considerations are mainly focused on the matching of the transistors’ pairs and the power transistor layout with minimum parasitic.

3.4.1. Transistor Matching

Transistor matching is a very important issue in analog circuit layout. The main purpose for layout matching is to reduce the mismatch offset arising from the fabrication process. Many circuit building blocks, such as current mirrors, input differential pairs and current mirror active loads involve matching with pair. There are two main techniques to match the transistors: inter-digitized technique and common-centroid technique. Figure 3.8 gives an exemplary symmetrical layout technique using common-centroid techniques. Device A and device B are laid out interleaved at the top, and are reversely order in the bottom. This gives the independence of process in both X and Y gradient directions. The dummy transistors are added at both sides to reduce lateral etching effect.
The layout of power transistor is critical for a good performance regulator since it introduces large parasitic in the feedback loop and draws large current from the supply to the output. First, to reduce the on-resistance ($R_{\text{on}}$), the device size (W/L ratio) has to be large and the minimum channel length is used. Second, to minimize the distributed gate resistance, multi-fingers structures should be used. The multi-fingers are arranged to form a transistor array in which the fingers are connected to interleaved source and drain metallization. This is then connected to higher level of metal by contacts and vias up to the top metal level. Figure 3.9 depicts the typical multi-fingers connection of the transistor array which not only reduces the gate resistance but it also reduces the junction capacitances [90, 91].

Fig. 3.8: Common centroid layout example.

3.4.2. Power Transistor Layout

The layout of power transistor is critical for a good performance regulator since it introduces large parasitic in the feedback loop and draws large current from the supply to the output. First, to reduce the on-resistance ($R_{\text{on}}$), the device size (W/L ratio) has to be large and the minimum channel length is used. Second, to minimize the distributed gate resistance, multi-fingers structures should be used. The multi-fingers are arranged to form a transistor array in which the fingers are connected to interleaved source and drain metallization. This is then connected to higher level of metal by contacts and vias up to the top metal level. Figure 3.9 depicts the typical multi-fingers connection of the transistor array which not only reduces the gate resistance but it also reduces the junction capacitances [90, 91].
In general, $R_{on}$ can be reduced by increasing the number of transistors in parallel configuration. However, at some point when the paralleled transistor number increases, $R_{on}$ does not continue to reduce and it tends to be saturated. This is mainly because the interconnect resistance becomes the main portion of $R_{on}$. To further reduce the $R_{on}$, some layout design techniques have been reported. Figure 3.10 shows a modified version of the multi-finger layout technique [92]. In this layout, wider metal layers are used to minimize the $R_{on}$. Nevertheless, a tradeoff exists between the width of metal layer and the number of contacts for drain/source.
Waffle transistor layout technique is another choice for the power transistor. Waffle transistor layout is depicted in Fig. 3.11. It achieves lower $R_{on}$ by using a mesh of horizontal and vertical poly gate stripes to divide the source and drain implant into an array of squares. After connecting these drain and source contact alternately, one can arrange four drains around each source and four sources around each drain [93]. The drains/sources are connected together by a diagonal stripes formed by metal layers. In general, the waffle layout offers a better packing density than that of the multi-finger layout [92]. Despite of the CMOS design rule (e.g. minimum metal width and spacing) of the metal layer, the drain/source diffusion area should be made larger to accommodate the metal layer. Moreover, in more recent CMOS process, the $R_{on}$ of the transistor is often dominated by the metallization. This causes the improvement of $R_{on}$ less significant.

Fig. 3.10: A modified multi-finger layout structure.
3.4.3. Metallization

In layout design for power transistor, the total width of the metal wire to supply and collect the large amount of load current also needs to be considered. The parasitic resistances of the metal layer ($R_M$) will cause additional voltage drop across the metal wire or bus of the regulator which may jeopardize the performance.

As discussed in [1], the general steps for passing output load current $I_L$ from $V_{DD}$ (or $V_{IN}$) to $V_O$ through the power transistor $M_P$ are listed as follows. (1) Steer $I_L$ laterally from $V_{DD}$ to a low-impedance plane (or planes) above power transistor $M_P$, (2) channel $I_L$ down vertically to $M_P$’s input terminal, (3) direct $I_L$ up vertically from $M_P$’s output terminal to another low-impedance plane (or planes), and (4) guide $I_L$ laterally to output pad $V_O$. To reduce the vertical resistance, the first-level metal should cover the entire ohmic surface area of each source and drain areas. As depicted in Fig. 3.12, the first-to-second level vias carry the current vertically to low-impedance second-level metal buses.
In sourcing current from the bonding pad to $M_P$ (or steering the current from $M_P$ to the bond pads), a lateral metal track above $M_P$ drives down (or “picks up”) parts of its current as it traverses across the IC. For instance, when sourcing current from the output terminal of $M_P$ (source region in Fig. 3.12) to the output pad, the total current in the lateral metal plane increases as more current from underlying current-carrying semiconductor regions is passed to the metal plane. If a constant metal width lateral metal plane is used, the current density throughout the plane is inconsistent. This will lead to current crowding and inefficient use of the available metal area. As a result, the lateral metal width should be designed to be increase when the total current passing through it increases. The best metallization strategy of second- to third-level metal planes is illustrated in Fig. 3.13 [1]. The third-level metal is drawn in triangle thus equal current-flux regions are formed to carry increasing or decreasing currents. To further reduce the metal resistance, multi-level metals are normally used for power routing as the higher levels of metal have a lower sheet resistance.

Fig. 3.12: Top view of a vertical-metallization strategy for a welled power MOSFET from the semiconductor interface to second-level metal planes [1].
Fig. 3.13: Top view lateral metallization strategy for a welled power MOSFET from second- to third-level metal planes and bond pads [1].
3.5. Summary

This Chapter first gives a review of conventional output capacitor LDO regulators. The stability and transient performances are discussed. Followed by the review of OCL-LDO regulators using different gain-stage topogies. For the topology with single-stage error amplifier and power transistor, the stability is easily achieved but at the price of limited regulator accuracy by the small loop gain. For the multi-stage error amplifier plus power transistor topology, the regulation accuracy is improved owing to an enhanced loop gain. However, the stability at low $I_L$ and the transient speed are sacrificed due to the additional high impedance node. Finally, the FVF based LDO regulator can give a low output impedance, simple structure and fast response characteristics.

In addition, the layout techniques for LDO regulator are discussed. Transistor matching, design techniques pertaining to the power transistor to achieve low $R_{on}$ are described.
CHAPTER 4

WIDE LOAD CAPACITANCE RANGE OCL-LDO REGULATOR: TYPE-I

In this Chapter, the Type-I wide CL range OCL-LDO regulator is introduced. The circuit structure, stability analysis, design methodology, and the other performances are discussed in detail.

4.1. Introduction

In System-on-Chip (SoC) environment pertaining to large scale digital circuits like DSP core(s) and memory banks, the effective supply line parasitic capacitance is large. To drive such circuits, the LDO regulator should have the ability to drive a wide load capacitance ($C_L$) range (few hundred pF to few nF) [38]. However, in most of the reported OCL-LDO regulator designs, they usually drive a maximum $C_L$ up to tens of pF or 100 pF [21, 22, 24, 27, 28, 30]. Few designs can drive relatively large $C_L$ [18, 23, 26, 29, 34].

In [18], a FVF topology is used as an output driver which gives a very fast speed with a recovering time of 0.54 ns. Since a quiescent current of 6 mA is used in this LDO regulator, it leads to unavoidable large quiescent power consumption. In addition, only a maximum $C_L$ of 600 pF is reported. A direct voltage spike detection technique is reported in [23] that can support a $C_L$ of 100 pF and 1 nF. Due to the LDO regulator utilizes a simple folded FVF topology, the loop gain is fairly limited. This in turn limits the regulation accuracy of the LDO regulator. In [26], an active
compensation scheme is realized in order to enable the LDO regulator to drive a $C_L$ up to 1 nF. However, several poles and zeros exist within the unity gain frequency ($\omega_{UGF}$), leading to complicated pole-zero tracking. Any mismatch between poles and zeros will contribute slower transient response. In [29], a current amplifier is adopted to multiply the Miller capacitor which can extend the $C_L$ driving capability to 1 nF. However, the design needs a large compensation capacitor (tens of pF) to ensure stable operation. This may lead to relatively larger silicon area and slower transient speed. A Dual-Summed Miller Frequency Compensation (DSMFC) technique is implemented in a FVF based LDO regulator topology [34]. The LDO regulator has been demonstrated in a very wide $C_L$ range. However, for the DSMFC network, the inverting driving transistor for the second Miller amplifier is biased by a high impedance current source with an open loop topology. To ensure a reliable dc operating region of the additional Miller stage, the power transistor has to be sized larger at the expense of larger silicon area so as to reduce the voltage swing at the Miller node. This will degrade the transient performances of the regulator.

In view of the need to support a wide $C_L$ range and good transient performance metrics under low quiescent power design objectives, new circuit techniques are demanded in the design of OCL-LDO regulators. In this report, two circuit techniques are proposed to extend the $C_L$ driving ability whilst maintain good transient performances. In this Chapter, the first type wide $C_L$ range LDO regulator uses the DSMFC technique but with a simpler structure and a reliable DC biased dual-summed Miller amplifier [94] is discussed. It can be drive a $C_L$ ranging from 10 pF to 10 nF with a total compensation capacitance ($C_C$) of 8 pF. The second type wide $C_L$ range LDO regulator will be discussed in subsequent Chapter.
4.2. Circuit Topology

The schematic of LDO regulator using DSMFC technique is shown in Fig. 4.1(a). It contains a folded FVF first gain stage, a non-inverting second gain stage and a power MOS transistor. The LDO regulator is compensated using a DSMFC block (dash enclosed area). It contains a standard Miller compensation capacitor ($C_{m1}$) and an additional Miller compensation stage ($C_{m2}$, $M_D$ and $R_X$). This realization permits a reliable DC operating point to be achieved in absence of high impedance node.

The control voltage for $M_1$ is generated through a symmetrical OTA amplifier which is shown in Fig. 4.1(b). Since the maximum load capacitor is in nF range, to reduce the settling time from overshoot, an overshoot reduction branch ($C_B$, $R_B$ and $M_7$) is implemented to increase the sinking current momentarily.
Fig. 4. (a) Schematic of the proposed FVF based LDO regulator with DSMFC ($v_{\text{fbin}}$, $v_{\text{fbout}}$ indicate the loop breaking point). (b) Control voltage ($V_{\text{CTRL}}$) generator.
4.3. **Stability and PSR Analysis and Discussions**

This section discusses the stability of the proposed LDO regulator using DSMFC technique. The small-signal mode, loop gain transfer function, poles and zeros locations, phase margin (PM), damping factor and gain margin (GM), and the sizing of the dual Miller compensation capacitors are investigated in detail.

4.3.1. **Small-Signal Model and Transfer Function**

The stability of proposed LDO regulator is examined using its small-signal model depicted in Fig. 4.2. It is obtained by breaking the feedback loop at the output branch as shown in Fig. 4.1(a). In the small-signal model, $g_{mi}$ denotes the transconductance whereas $R_i$ and $C_i$ are the equivalent output resistance and lumped output parasitic capacitance of the i-th gain stage, respectively. $C_{m1}$ and $C_{m2}$ are the 1\textsuperscript{st} and 2\textsuperscript{nd} Miller compensation capacitors. $R_O$ is the effective output resistance which includes the output resistance of power transistor and the loading resistance $R_L$. $C_L$ is the load capacitance which has a value ranging from 10 pF to 10 nF.

![Fig. 4.2: Small-signal model of the proposed FVF LDO regulator.](image-url)
The loop gain transfer function is derived with the following assumptions: (i) \(C_D \ll C_2 \ll C_m1, C_m2\) and \(C_L\); (ii) \(g_{m1}R_1, g_{m2}R_2\) and \(g_{md}R_D \gg 1\). It is obtained and expressed by (4.1), where \(A_{dc}\) is the dc loop gain and \(z_1, z_2, z_3\) are the three zeros.

\[
T(s) = \frac{v_{f_{out}}}{v_{f_{in}}} = -\frac{A_{dc}}{1 + as + bs^2 + cs^3 + ds^4} \left(1 + \frac{s}{z_1} \right) \left(1 + \frac{s}{z_2} \right) \left(1 + \frac{s}{z_3} \right)
\]

\[
A_{dc} = g_{m1}g_{m2}g_{mp}R_1R_2R_O, \quad z_1 = -\frac{1}{C_m2R_D},
\]

\[
z_2 \approx \frac{-C_m1 - 2R_2\sqrt{C_m1C_2g_{m2}g_{mp}}}{2C_m1C_2R_2}, \quad z_3 \approx \frac{-C_m1 + 2R_2\sqrt{C_m1C_2g_{m2}g_{mp}}}{2C_m1C_2R_2},
\]

\[
a = C_m2g_{md}R_DR_1 + C_m1g_{m2}g_{mp}R_1R_2R_O + C_LR_O,
\]

\[
b = C_m2g_{md}R_DR_1(C_2R_2 + C_LR_O) + C_m1C_m2g_{m2}g_{mp}R_DDR_2R_O,
\]

\[
c = C_m2C_2g_{md}R_DDR_2R_O + (g_{md}R_O + 1)C_m1C_m2C_2R_DDR_2R_O + C_m1C_m2C_LR_DR_1R_O,
\]

\[
d = C_m1C_m2C_2C_LR_DDR_1R_2R_O.
\]

(4.1)

Based on the design parameters, \(z_{2,3}\) locate at high frequencies. Thus it can be ignored in the stability analysis. In addition, the loop gain transfer function has two real poles (\(p_{3dB}, p_2\)). As such, it can be simplified in the form as

\[
T(s) = -\frac{A_{dc}}{\left(1 + \frac{s}{p_{3dB}}\right) \left(1 + \frac{s}{p_2}\right) \left(1 + \frac{c}{b} + \frac{d}{b}s^2\right)} \left(1 + \frac{s}{z_1}\right)
\]

(4.2)
4.3.2. Poles and Zero Locations

Since the $C_L$ varies from 10 pF to 10 nF with the load current $I_L$ switching between 0 and 50 mA, the stability of the LDO regulator is discussed at six different cases that deal with the $C_L$ corners at different $I_L$. They are given as follows: (1) Large $C_L$ with low $I_L$, (2) Large $C_L$ with moderate $I_L$, (3) Large $C_L$ with high $I_L$, (4) Small $C_L$ with low $I_L$, (5) Small $C_L$ with moderate $I_L$, (6) Small $C_L$ with high $I_L$.

Based on (4.1) and (4.2), the poles and zeros locations for six cases are summarized in Table 4.1 and their relative locations are shown in Fig. 4.3(a) and Fig. 4.3(b) for large and small $C_L$, respectively. The loop gain transfer function shows that the first case denotes the system with four real poles whereas the other five cases denote the system having two real poles plus one pair of complex poles. Each case is explained as follows:

**Case 1: Large $C_L$ with low $I_L$**

In this case, both power transistor’s output resistance ($R_{dsp}$) and the equivalent load circuit resistance ($R_L$) are high. As a result, $R_O \approx 1/g_{m1}$. Due to a small bias current in $M_1$, $R_O$ is still fairly large (around 17 kΩ). It forms a low frequency dominant pole with the large $C_L$. $p_2$ is located at a lower frequency than that of $z_1$, contributing a partial cancellation effect. In addition, due to the DSMFC, $p_3$ is pushed to a higher frequency by an extra frequency quantifying term, $g_{md}/C_{m1}$. As for $p_4$, the gain of the last stage is small due to small $g_{mp}$. Thus the Miller effect arising from the $C_{gd}$ of the power transistor is negligible, which results in a small $C_2$. Therefore, $p_4$ is also located at a high frequency.

**Case 2: Large $C_L$ with moderate $I_L$**

Due to large $g_{mp}$ and moderate $R_O$, the loop gain is the highest in this range and the stability of the LDO regulator is at its worst condition. $p_{3dB}$ is formed by the Miller
<table>
<thead>
<tr>
<th>Parameter</th>
<th>$z_1$</th>
<th>$P_{3dB}$</th>
<th>$p_2$</th>
<th>$p_3^*$</th>
<th>$p_4^*$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>(Case 1)</strong> Large $C_L$/Low $I_L$</td>
<td>$-\frac{1}{C_m R_D}$</td>
<td>$-\frac{1}{C_L R_O}$</td>
<td>$-\frac{1}{C_m g_{md} R_R R_D}$</td>
<td>$-\left(\frac{g_{md}}{C_m} + \frac{g_{mp} g_{mp} R_2}{C_L}\right)$</td>
<td>$-\frac{1}{C_2 R_2}$</td>
</tr>
<tr>
<td><strong>(Case 2)</strong> Large $C_L$/Moderate $I_L$</td>
<td>$-\frac{1}{C_m R_D}$</td>
<td>$-\frac{1}{C_m g_{md} R_R R_D}$</td>
<td>$-\frac{C_m g_{mp} R_2}{C_m g_{mp} R_R R_D + C_m g_{md} R_D}$</td>
<td>$\frac{g_{mp} R_2}{\sqrt{C_2 C_L}} + \frac{g_{md}}{C_m C_2 R_2}$</td>
<td></td>
</tr>
<tr>
<td><strong>(Case 3)</strong> Large $C_L$/High $I_L$</td>
<td>$-\frac{1}{C_m R_D}$</td>
<td>$-\frac{1}{C_m g_{md} R_R R_D}$</td>
<td>$-\left(\frac{g_{md}}{C_m} + \frac{g_{mp} R_2}{C_m R_D}\right)$</td>
<td>$\sqrt{\frac{g_{mp} g_{mp}}{C_2 C_L}}$</td>
<td></td>
</tr>
<tr>
<td><strong>(Case 4)</strong> Small $C_L$/Low $I_L$</td>
<td>$-\frac{1}{C_m R_D}$</td>
<td>$-\frac{1}{C_m g_{md} R_R R_D}$</td>
<td>$-\left(\frac{g_{md}}{C_m} + \frac{g_{mp} R_2}{C_m R_D}\right)$</td>
<td>$\sqrt{\frac{g_{mp} g_{mp}}{C_2 C_L}}$</td>
<td></td>
</tr>
<tr>
<td><strong>(Case 5)</strong> Small $C_L$/Moderate $I_L$</td>
<td>$-\frac{1}{C_m R_D}$</td>
<td>$-\frac{1}{C_m g_{md} R_R R_D}$</td>
<td>$-\frac{1}{C_m R_D}$</td>
<td>$\sqrt{\frac{g_{mp} g_{mp}}{C_2 C_L}}$</td>
<td></td>
</tr>
<tr>
<td><strong>(Case 6)</strong> Small $C_L$/High $I_L$</td>
<td>$-\frac{1}{C_m R_D}$</td>
<td>$-\frac{1}{C_m g_{md} R_R R_D}$</td>
<td>$-\left(\frac{g_{md}}{C_m} + \frac{g_{mp} R_2}{C_m R_D}\right)$</td>
<td>$\sqrt{\frac{g_{mp} g_{mp}}{C_2 C_L}}$</td>
<td></td>
</tr>
</tbody>
</table>

* $p_3$ and $p_4$ form a pair of complex poles except for large $C_L$ with low $I_L$ condition.
compensation capacitor $C_{m1}$. More importantly, similar to Case 1, an additional term, $g_{md}/(C_{m1}C_2R_2)$, is generated for defining complex poles’ frequency in the DSMFC scheme. As a result, the complex pole pair $|p_{3,4}|$ are shifted to a higher frequency which ensures the stability of the regulator is achieved.

**Case 3: Large $C_L$ with high $I_L$**

In this case, $R_O$ is approaching to its minimum value because of small $R_{dsp}$ and small $R_L$. This leads to a small gain for the power transistor gain stage. The two Miller compensation effects are close to each other and form the dominant pole together. The second pole and zero ($z_1$ is around 2 times of $p_2$) exhibit a good cancellation. The complex poles are located at higher frequency due to large $g_{mp}$.

*Fig. 4.3: Loop gain of the proposed FVF LDO regulator with poles and zero locations for (a) large $C_L$, (b) small $C_L$.  

$p_{i_l}, z_{i_l}, p_{i_m}, z_{i_m}, p_{i_h}, z_{i_h}$ represent the $i^{th}$ pole and zero for low, moderate and high load current respectively.
**Case 4: Small \( C_L \) with low \( I_L \)**

Due to small \( C_L \), \( C_L R_O \) no longer forms a low frequency pole. The dominant pole is governed by two Miller compensation capacitors (\( C_{m1} \) and \( C_{m2} \)). A good pole and zero cancellation is also achieved in this case. Similar to Case 2, the complex poles are shifted to a higher frequency by the additional term generated by the DSMFC. The stability of the LDO regulator is ensured.

**Case 5: Small \( C_L \) with moderate \( I_L \)**

Similar to Case 2, the dominant pole is created by the standard Miller capacitor (\( C_{m1} \)). The complex poles are located at high frequency because of the small \( C_L \). Thus they will not affect the stability of the LDO regulator.

**Case 6: Small \( C_L \) with high \( I_L \)**

Similar to Case 5, it is apparent that the stability of the LDO regulator at this condition can easily be achieved due to large \( g_{mp} \) and small \( C_L \).

With the DSMFC technique, the dominant pole is formed through the summing Miller effect which offers better stability. Besides, when comparing with Single Miller Compensation (SMC) counterpart, the DSMFC also shifts the non-dominant pole(s) to a higher frequency, especially under the following three conditions: (i) large \( C_L \) with low \( I_L \), (ii) large \( C_L \) with moderate \( I_L \), and (iii) small \( C_L \) with low \( I_L \). Since the DSMFC technique addresses the conservative stability issue for both small and large \( C_L \), the proposed LDO regulator can achieve driving capability for a wide load capacitance range across the whole load current range.

Figure 4.4(a) and 4.4(b) depict the open-loop gain and phase responses at \( I_L = 0 \), 0.5 mA, 5 mA, and 50 mA for \( C_L = 10 \text{ nF} \) and \( C_L = 10 \text{ pF} \), respectively. It can be observed that the simulated results match with the analysis. It also demonstrates that
the proposed FVF LDO regulator can achieve stability for both large and small \( C_L \) corners at different \( I_L \).

**Fig. 4.4:** Simulated open-loop gain and phase responses at different \( I_L \) for (a) \( C_L = 10 \text{ nF} \) and (b) \( C_L = 10 \text{ pF} \).
The PM, GM and unity gain frequency across the whole $C_L$ range with different $I_L$ are shown in Fig. 4.5. It can be observed that the LDO regulator with DSMFC technique achieves a minimum PM of $50^\circ$ and a minimum GM of 8 dB. For benchmark comparison, the SMC for this LDO regulator topology without using the second Miller amplifier is applied. The total compensation capacitance in the proposed LDO regulator and the SMC LDO regulator are sized to be the same (8 pF). Figure 4.6 depicts the PM, GM and unity gain frequency simulation results. As can be seen from Fig. 4.6(a), based on a $50^\circ$ PM, the SMC regulator is stable to support a load capacitor ranging from 10 pF to 250 pF. Moreover, when comparing the unity gain frequency simulation results in Fig. 4.5(c) and Fig. 4.6(c), the proposed LDO regulator using the DSMFC technique provides a larger unity gain frequency with respect to that of SMC LDO regulator. This suggests that the speed of the LDO regulator will be faster in the proposed LDO regulator.

Based on the above analysis and simulation results, the proposed FVF LDO regulator using DSMFC technique is able to maintain stable operation over the whole $C_L$ range of 10 pF – 10 nF under the load current varying from 0 to 50 mA. With respect to the SMC counterpart, it achieves a wider $C_L$ range at the same time a larger unity gain frequency.
Fig. 4.5: Simulated (a) Phase Margin, (b) Gain Margin and (c) Unity Gain Frequency as a function of $C_L$ at different $I_L$ using DSMFC.

Fig. 4.6: Simulated (a) Phase Margin, (b) Gain Margin and (c) Unity Gain Frequency as a function of $C_L$ at different $I_L$ using SMC.
4.3.3. Phase Margin under Different $C_L$

As can be seen in Fig. 4.5(a), at small $I_L$ condition, the PM plot shows a “quadratic” behavior. When $C_L$ increases, the PM drops from $83^\circ$ to around $60^\circ$ and then increases again. If $C_L$ continues to increase, the PM will drop again. The phenomenon is due to shifting of the pole when $C_L$ varies from small to large values. The analysis can be divided into two regions: (i) complex pole region for small $C_L$ and (ii) real pole region for large $C_L$.

**Region i:** In this region, owing to small $C_L$, the dominant pole $p_{3dB}$ is formed by the two Miller compensation capacitors ($C_{m1}$ and $C_{m2}$). It gives a $C_L$ independent unity gain frequency $\omega_{UGF}$ as

$$\omega_{UGF} = \frac{g_{m1}g_{m2}g_m R_2 R_O}{C_{m2} g_m R_1 R_1 + C_{m1} g_{m2} g_m R_1 R_O}$$

(4.3)

In addition, the loop system gives a pair of complex poles which are given by

$$|p_{34}| = \sqrt{\frac{g_{m2} g_m}{C_2 C_L} + \frac{g_m}{C_{m1} C_2 R_1}}$$

(4.4)

From (4.4), it can be seen that the location of the complex poles is inversely proportional to $C_L$. As $C_L$ increases, the complex poles’ frequency decreases and appears to be closer to $\omega_{UGF}$. As a consequence, the PM is reduced and the stability of LDO regulator becomes worse. This explains why the PM plot in Fig. 4.5(a) shows a continuous drop first when $C_L$ is less than 250 pF.

**Region ii:** For large $C_L$, the output capacitor also plays a role in the dominant pole formation. The dominant pole is given as

$$p_{3dB} = \frac{1}{C_{m2} g_m R_2 R_1 + C_{m1} g_{m2} g_m R_1 R_2 R_O + C_L R_O}$$

(4.5)
which leads to a $C_L$ dependent $\omega_{UGF}$ as follows:

$$\omega_{UGF} = \frac{g_{m1}g_{m2}g_{mp}R_1R_2R_O}{C_m g_{md}R_p+g_{m1}g_{m2}g_{mp}R_1R_2R_O+C_2R_O}$$  \hspace{1cm} (4.6)

Since the zero $z_1$ generated from the DSMFC is fixed at $1/C_m R_D$ (4.1) and the second pole ($p_2$) locates at a lower ($g_{md} R_1$ times) frequency, the loop phase response gives a small peak around the zero location. Based on this reason, when $\omega_{UGF}$ continues to reduce as $C_L$ increases, the PM will increase and then drop again, depending on the relative location of $\omega_{UGF}$ and the fixed zero $z_1$.

### 4.3.4. Damping Factor and Gain Margin under Different $C_L$

Damping factor is critical for the LDO regulator stability when a pair of complex poles exist in the loop gain transfer function (case 2 to case 6 in Table 4.1). Consider the second-order terms in (4.2) with a standard form as

$$1 + \frac{c}{b}s + \frac{d}{s}s^2 = 1 + \left(\frac{2\zeta}{\omega_o}\right)s + \left(\frac{s}{\omega_o}\right)^2$$

\hspace{1cm} (4.7)

where $\zeta$ is the damping factor and $\omega_o$ is the frequency of the complex poles.

Although the DSMFC increases the frequency of the complex poles ($\omega_o$) which in turn improves the PM and GM, the $\zeta$ of the complex poles should be designed properly to avoid large frequency peaking and maintain a good GM. If it is assumed that the second pole $p_2$ and the zero $z_1$ generated by the DSMFC cancel each other, based on [25], the relationship between $\zeta$ and PM as well as $\zeta$ and GM in a second-order system is approximately as follows:
\[ PM \approx 90^\circ - \tan^{-1}\left(\frac{2\zeta \Omega_O}{\Omega_{UGF}}\right) \]  

(4.8)

\[ GM \approx 20 \times \log\left(\frac{2\zeta \Omega_O}{\Omega_{UGF}}\right) \]  

(4.9)

From (4.8) and (4.9), a large \( \zeta \) increases the GM but it gives a large negative phase shift which reduces the PM. On the other hand, a small \( \zeta \) reduces the GM and makes a sharp phase drop which can lead to a 0\(^\circ\) PM.

Based on transfer function in (4.1), the general expression for the \( \zeta \) in the second-order system defined in (4.7) is obtained as

\[ \zeta = \frac{1}{2} \left( C_{2g_m} R_{r1} R_2 + C_{m1} R_1 \right) C_L + \left( g_{m1} R_{r1} + 1 \right) C_{m1} C_2 R_2 \]

\[ C_{m1} R_1 R_2 \sqrt{C_2 C_{Ls} g_{mp}} \]

(4.10)

It is noted that the GM without taking log function is \( 2\zeta \Omega_O/\Omega_{UGF} \). Therefore, the \( \zeta \) and \( 2\zeta \Omega_O/\Omega_{UGF} \) for 5 cases exhibiting a complex pole pair (case 2 – case 6 in Table 4.1) are summarized in Table 4.2. For case 1 in Table 4.1 (large \( C_L \), low \( I_L \)), the system displays four real poles, thus it is not included in Table 4.2 and the respective analysis.

From Table 4.2, when \( C_L \) increases, the observation is in the following. (i) For low \( I_L \) and small \( C_L \) (case 4), \( \zeta \) increases. (ii) For moderate \( I_L \) (case 2 and case 5), \( \zeta \) will reduce first and then increase again. (iii) For high \( I_L \) (case 3 and case 6), \( \zeta \) decreases.

Therefore, the minimum \( \zeta \) (\( \zeta_{(\text{min})} \)) for low \( I_L \) occurs at \( C_L = 10 \) pF whereas for high \( I_L \), \( \zeta_{(\text{min})} \) occurs at \( C_L = 10 \) nF. For moderate \( I_L \), \( \zeta_{(\text{min})} \) occurs at middle \( C_L \) range. The value of \( \zeta_{(\text{min})} \) can be approximated as

\[ \zeta_{(\text{min})} \approx \frac{1}{C_{m1} R_1} \sqrt{\frac{C_{m1} \left( C_{2g_m} R_2 + C_{m1} R_1 \right)}{g_{m2} g_{mp} R_2}} \]

(4.11)
Based on the above analytical expressions, the \( \zeta \) for different \( I_L \) conditions and their respective \( C_L \) location (\( C_L, \zeta \)) are summarized in Table 4.3. They are governed by the design parameters in which the denoted symbols have their usual meanings.

Consider GM of the LDO regulator depicted in Table 4.2, when \( C_L \) increases, it follows the same trend as that of \( \zeta \) under low, moderate and high \( I_L \) cases. Therefore, (i) At low \( I_L \), the minimum GM (\( \text{GM}_{\text{min}} \)) occurs at \( C_L = 10 \) pF. (ii) At high \( I_L \), \( \text{GM}_{\text{min}} \) occurs at \( C_L = 10 \) nF. (iii) At moderate \( I_L \), \( \text{GM}_{\text{min}} \) occurs at middle \( C_L \) range. The \( \text{GM}_{\text{min}} \) for three different \( I_L \) conditions and their respective \( C_L \) location (\( C_L, \text{GM}_{\text{min}} \))

\[
\zeta (C_L \uparrow) = \alpha \sqrt{\frac{C_L}{C_2 g_m 2 \mu p}} \\
\text{GM}^* (C_L \uparrow) = \frac{\beta (C_2 g_m R_S + C_m)}{C_2 g_m 2 \mu p} \\
\]

\[
\begin{array}{|c|c|c|}
\hline
\text{Parameter} & \zeta (C_L \uparrow) & \text{GM}^* (C_L \uparrow) \\
\hline
\text{(Case 2)} & \alpha \sqrt{\frac{C_L}{C_2 g_m 2 \mu p}} & \frac{\beta (C_2 g_m R_S + C_m)}{C_2 g_m 2 \mu p} \uparrow \\
\text{Large } C_L \text{ Moderate } I_L & \uparrow & \uparrow \\
\hline
\text{(Case 3)} & \frac{1}{2 R_S} \sqrt{\frac{C_2}{C_4 g_m 2 \mu p}} & \frac{C_m}{C_2 g_m 2 \mu p} \downarrow \\
\text{Large } C_L \text{ High } I_L & \downarrow & \downarrow \\
\hline
\text{(Case 4)} & \frac{1}{2 R_S} \sqrt{\frac{C_2}{C_4 g_m 2 \mu p}} & \frac{\beta (C_2 g_m R_S + C_m)}{C_2 g_m 2 \mu p} \downarrow \\
\text{Small } C_L \text{ Low } I_L & \downarrow & \downarrow \\
\hline
\text{(Case 5)} & \frac{1}{2 R_S} \sqrt{\frac{C_2}{C_4 g_m 2 \mu p}} & \frac{C_4}{C_2 g_m 2 \mu p} \downarrow \\
\text{Small } C_L \text{ Moderate } I_L & \downarrow & \downarrow \\
\hline
\text{(Case 6)} & \frac{1}{2 R_S} \sqrt{\frac{C_2}{C_4 g_m 2 \mu p}} & \frac{C_m}{C_2 g_m 2 \mu p} \downarrow \\
\text{Small } C_L \text{ High } I_L & \downarrow & \downarrow \\
\hline
\end{array}

\[
\uparrow \text{and } \downarrow \text{ indicates the increase or decrease of } \zeta \text{ and GM when } C_L \text{ increases, respectively.} \\
\text{* GM without taking log function.} \\
\text{# } \alpha = \frac{(C_2 g_m R_S + C_m)}{2 C_m 2 \mu p}, \beta = \sqrt{1 + \frac{C_4 g_m 2 \mu p}{C_2 g_m 2 \mu p} \frac{R_S}{R_S}} \\
\]

\[
C_{L, \zeta_{\text{min}}} \approx \frac{C_4 C_2 R_S}{C_2 g_m 2 \mu p R_S + C_m R_S} \quad (4.12)
\]

Based on the above analytical expressions, the \( \zeta_{\text{min}} \) for different \( I_L \) conditions and their respective \( C_L \) location (\( C_L, \zeta_{\text{min}} \)) are summarized in Table 4.3. They are governed by the design parameters in which the denoted symbols have their usual meanings.

Consider GM of the LDO regulator depicted in Table 4.2, when \( C_L \) increases, it follows the same trend as that of \( \zeta \) under low, moderate and high \( I_L \) cases. Therefore, (i) At low \( I_L \), the minimum GM (\( \text{GM}_{\text{min}} \)) occurs at \( C_L = 10 \) pF. (ii) At high \( I_L \), \( \text{GM}_{\text{min}} \) occurs at \( C_L = 10 \) nF. (iii) At moderate \( I_L \), \( \text{GM}_{\text{min}} \) occurs at middle \( C_L \) range. The \( \text{GM}_{\text{min}} \) for three different \( I_L \) conditions and their respective \( C_L \) location (\( C_L, \text{GM}_{\text{min}} \))
are also summarized in Table 4.3. Turning to the GM plot of the proposed LDO regulator in Fig. 4.5(b), at \( I_L = 0 \), the minimum GM location is at \( C_L = 10 \text{ pF} \). On the other hand, at \( I_L = 5 \) and 50 mA, the minimum GM location is at \( C_L = 10 \text{ nF} \). This matches the GM\(_{\text{min}}\) location analysis for low and high \( I_L \) conditions, respectively.

At moderate \( I_L \), through derivation and Binomial approximations, the minimum GM (without taking log function) is approximated as

\[
GM_{\text{min}} \approx \left( \frac{C_2 g_{md} R_2 + C_{m1}}{C_2 g_{m1} R_2} \right) + \sqrt{\frac{2 g_{md} (C_2 g_{md} R_2 + C_{m1})}{C_2 g_{m1}^2 g_{m2} g_{mp} R_2^2 R_O}} \tag{4.13}
\]

which occurs at

\[
C_{L,GM(\text{min})} \approx C_{m1} R_2 \sqrt{\frac{2 C_2 g_{m2} g_{mp}}{g_{md} R_O (C_2 g_{md} R_2 + C_{m1})}} \tag{4.14}
\]

To demonstrate the analysis with an example, at \( I_L = 0.5 \text{ mA} \), the design parameters are given as follows: \( C_{m1} = 4 \text{ pF}, C_2 = 1.04 \text{ pF}, g_{m2} = 239 \mu \text{S}, g_{mp} = 9 \text{ mS}, g_{md} = 31\mu \text{S}, R_2 = 81 \text{ k\Omega}, \) and \( R_O = 540 \text{ \Omega} \). Using (4.14), it gives a \( C_{L,GM(\text{min})} \) of 2.06 nF. The GM plot in Fig. 4.5(b) also shows that the minimum GM occurs around \( C_L = 2 \text{ nF} \). This validates that the analytical expression for the minimum GM location correlates well with the simulation result.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>$\zeta_{(\text{min})}$</th>
<th>$CL_{\zeta}(\text{min})$</th>
<th>$GM_{(\text{min})}^*$</th>
<th>$CL_{\text{GM(min)}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Low $I_L$</strong></td>
<td>$\frac{1}{2R_1} \sqrt{\frac{C_{L_{\text{min}}}}{C_{2}g_{m2}g_{mp}}}$</td>
<td>$CL_{(\text{min})}$ #</td>
<td>$\frac{C_{m2}g_{md}R_D + C_{m1}g_{m2}g_{mp}R_{2}R_{O}}{C_{2}g_{m1}g_{m2}g_{mp}R_{2}^{2}R_{O}} \sqrt{1 + \frac{C_{L_{\text{min}}}g_{md}}{C_{m1}g_{m2}g_{mp}R_{2}^{2}}}$</td>
<td>$CL_{(\text{min})}$ #</td>
</tr>
<tr>
<td><strong>Moderate $I_L$</strong></td>
<td>$\frac{1}{C_{m1}R_{O}} \sqrt{\frac{C_{m1}(C_{2}g_{md}R_{2}R_{O} + C_{m2}R_{O})}{g_{m2}g_{mp}R_{2}}}$</td>
<td>$\frac{C_{m1}R_{2}}{C_{2}g_{m1}R_{2} + C_{m2}R_{O}} + \frac{2g_{md}(C_{2}g_{md}R_{2} + C_{m1})}{C_{2}g_{m1}R_{2}} \sqrt{\frac{C_{m1}g_{m2}g_{mp}R_{2}^{2}R_{O}}{g_{md}R_{O}(C_{2}g_{md}R_{2} + C_{m1})}}$</td>
<td>$C_{m1}R_{2}$</td>
<td>$\frac{2C_{m2}g_{md}g_{mp}}{g_{md}R_{O}(C_{2}g_{md}R_{2} + C_{m1})}$</td>
</tr>
<tr>
<td><strong>High $I_L$</strong></td>
<td>$\frac{1}{2R_{O}} \sqrt{\frac{C_{2}}{C_{L_{\text{max}}}g_{m2}g_{mp}}}$</td>
<td>$CL_{(\text{max})}$ #</td>
<td>$\frac{C_{m1}C_{m2}g_{md}R_D + C_{m1}g_{m2}g_{mp}R_{2}R_{O}}{C_{L_{\text{max}}}g_{m2}g_{mp}R_{2}^{2}R_{O}}$</td>
<td>$CL_{(\text{max})}$ #</td>
</tr>
</tbody>
</table>

# $C_{L_{\text{min}}} = 10 \text{ pF}$, $C_{L_{\text{max}}} = 10 \text{ nF}$. * $GM_{(\text{min})}$ without taking log function.
4.3.5. Sizing of Dual Miller Compensation Capacitors

The dimensions of the two Miller compensation capacitors \((C_{m1} \text{ and } C_{m2})\) are depending on the gain of the main loop and the dual-summed amplifier. To analyze the influence, two cases of \(C_{m1} \text{ and } C_{m2}\) are discussed and compared with the nominal case. It is assumed that the nominal case is at \(C_{m1} = C_{m2}\) and the total sum is kept at a constant (8 pF in this design).

**Case I**: \(C_{m1} > C_{m2}\). For large \(C_L\) under low \(I_L\) (case 1 in Table 4.1), a large \(C_{m1}\) degrades the stability of the LDO regulator. This is because large \(C_{m1}\) gives a lower frequency \(p_3\) that leads to a poor PM. Under moderate \(I_L\) (case 2 in Table 4.1), the Miller effect is strong because of large \(C_{m1}\). The stability of LDO regulator is improved. For small \(C_L\) under low and moderate \(I_L\) (case 4 and case 5 in Table 4.1), large \(C_{m1}\) improves the stability of the LDO regulator due to a stronger pole splitting effect. This occurs when the gain of the second stage plus the power transistor gain is larger than the gain of the dual-summed amplifier, which is especially true under low and moderate \(I_L\). As for high \(I_L\) for both small and large \(C_L\) (case 3 and case 6 in Table 4.1), the stability improvement is small due to a small power transistor gain. This results in a similar Miller compensation effect for \(C_{m1}\) and \(C_{m2}\).

**Case II**: \(C_{m1} < C_{m2}\). Under this case, the LDO regulator stability is in opposite effect from those described in Case I \((C_{m1} > C_{m2})\). Therefore, it is not repeated here.

Based on the analysis in Case I and Case II, the relative PM and GM with reference to the nominal case of \(C_{m1} = C_{m2}\) is summarized in Table 4.4 when \(C_{m1}\) and \(C_{m2}\) change their values in different combinations. The symbol “＋” represents PM and GM increase whereas the symbol “－” represents PM and GM decrease with respect to the nominal case that \(C_{m1} = C_{m2}\).

Table 4.5 gives the simulated PM and GM for the capacitor pair \((C_{m1}, C_{m2})\) which
corresponds to the design values of (5 pF, 3 pF), (4 pF, 4 pF) and (3 pF, 5 pF). For example one, at \(I_L = 0\) mA (low \(I_L\)) and \(C_L = 10\) pF (small \(C_L\)), when \(C_{m1} = 5\) pF, \(C_{m2} = 3\) pF, both PM and GM are larger than that of nominal case (\(C_{m1} = 4\) pF, \(C_{m2} = 4\) pF).

For example two, at \(I_L = 0\) mA (low \(I_L\)) and \(C_L = 10\) nF (large \(C_L\)), when \(C_{m1} = 5\) pF, \(C_{m2} = 3\) pF, both PM and GM are smaller than the nominal case. This confirms that the simulation results on the size of \(C_{m1}\) and \(C_{m2}\) correlate well with the expected behavior as indicated in Table 4.4.

**Table 4.4 Relative PM and GM for Different \(C_{m1} & C_{m2}\) Combinations with Reference to Nominal Case**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>(C_{m1} &gt; C_{m2})</th>
<th>(C_{m1} &lt; C_{m2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_L) Low</td>
<td>Moderate</td>
<td>High</td>
</tr>
<tr>
<td>Large (C_L)</td>
<td>–</td>
<td>+</td>
</tr>
<tr>
<td>Small (C_L)</td>
<td>+</td>
<td>+</td>
</tr>
</tbody>
</table>

**Table 4.5 PM and GM for Different \(C_{m1} & C_{m2}\) Combinations**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>(C_{m1} = 5) pF (C_{m2} = 3) pF</th>
<th>(C_{m1} = 4) pF (C_{m2} = 4) pF</th>
<th>(C_{m1} = 3) pF (C_{m2} = 5) pF</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_L) (mA)</td>
<td>0</td>
<td>0.5</td>
<td>50</td>
</tr>
<tr>
<td>10 pF (PM)</td>
<td>84</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>10 pF (GM)</td>
<td>9</td>
<td>21</td>
<td>–</td>
</tr>
<tr>
<td>10 nF (PM)</td>
<td>45</td>
<td>61</td>
<td>87</td>
</tr>
<tr>
<td>10 nF (GM)</td>
<td>40</td>
<td>12</td>
<td>14</td>
</tr>
</tbody>
</table>

GM is too high and it is out of the simulation range.
4.3.6. Power Supply Rejection Analysis

The power supply rejection of LDO regulator indicates the ability to immune against the supply variation. Figure 4.7 depicts the schematic of the LDO regulator with power supply noise injection paths (in Red arrows).

Fig. 4.7 Schematic of the LDO regulator with power supply noise injection paths.
The PSR of the regulator is analyzed in low, moderate and high frequency ranges. To simplify the analysis, the loop gain of the regulator in (4.2) is assumed to be one-pole system within unity-gain frequency (UGF), which can be expressed as

\[ T(s) = \frac{A_{dc}}{1 + s/p_{-3dB}}. \]

Thus, the regulated output impedance can be expressed as

\[
\begin{align*}
Z_{reg} &= \frac{Z_{out} \parallel R_{dp}}{T(s)} \\
&= \frac{Z_{out} \parallel R_{dp}}{A_{dc}} (1 + s/p_{-3dB}) \frac{Z_{out} \parallel R_{dp}}{T(s)} = \frac{Z_{out} \parallel R_{dp}}{A_{dc}} (1 + s/p_{-3dB})
\end{align*}
\]

(4.15)

where \( Z_{out} = R_L \parallel (1/sC_L) \) and stands for the effective load impedance, \( R_{dp} \) is the output impedance of the power transistor [95]. The PSR of the LDO regulator is analyzed in three regions: (i) low frequency, (ii) moderate frequency and (iii) high frequency. It is assumed the supply noise is \( \Delta V_{DD} \).

(i) At low frequency, for path 1, assume \( M_{11} \sim M_{14} \) and \( M_{16} \sim M_{17} \) are matched with each other, the noise for \( V_{CTRL} \) can be expressed as

\[
\Delta V_{CTRL} \approx \frac{(R_{d17} \parallel R_{d14})/A_{CTRL}}{(R_{d17} \parallel R_{d14})/A_{CTRL} + R_{d14}} \Delta V_{DD} \\
\approx \frac{R_{d17} \parallel R_{d14}}{A_{CTRL} R_{d14}} \Delta V_{DD} \\
= \frac{\Delta V_{DD}}{g_{mv} R_{d14}}
\]

(4.16)

After \( \Delta V_{CTRL} \) is applied to \( M_1 \), it goes through the first and second gain stage, the noise at node \( N_2 \) due to path 1 can be expressed as

\[
\Delta V_{N_2-1} = -g_{m1} R_{ds} g_{m2} R_{ds} \Delta V_{CTRL} \\
= -\frac{g_{m1} R_{ds} g_{m2} R_{ds}}{g_{mv} R_{d14}} \Delta V_{DD}
\]

(4.17)
where $g_{mi}$ and $R_i$ stands for the transconductance of transistor $M_i$ and equivalent output resistance of the $i$-th gain stage as that in Section 4.3.1.

For path 2, the supply noise will change the source voltage of $M_2$ and generate a noise current, this current will be mirrored to $N_2$ and generate a noise voltage at $N_2$ as

$$
\Delta V_{N2-2} = g_{m2}R_2\Delta V_{DD}
$$

(4.18)

For path 3, since $V_{B1}$ can be tracked with $V_{IN}$ due to the diode transistor $M_{B1}$, thus the only way for the supply noise injecting into $N_2$ is due to limited $R_{ds5}$ which can be expressed as

$$
\Delta V_{N2-3} = \frac{R_{ds4}}{R_{ds4} + R_{ds5}} \Delta V_{DD}
$$

(4.19)

For path 4, at low frequency, the capacitor $C_{m1}$ has a very high impedance, supply noise cannot be coupled to $N_1$ leading to a zero noise contribution at $V_{OUT}$ from path 4.
As such, the total noise at $N_2$ can be expressed as

$$
\Delta V_{N2} = \Delta V_{N2-1} + \Delta V_{N2-2} + \Delta V_{N2-3}
$$

$$
= -\frac{g_{mi}R_1 g_{m2}R_2}{g_{m9}R_{ds14}} \Delta V_{DD} + g_{m2}R_2\Delta V_{DD} + \frac{R_{ds4}}{R_{ds4} + R_{ds5}} \Delta V_{DD}
$$

$$
\approx g_{m2}R_2\Delta V_{DD} - \frac{g_{mi}R_1 g_{m2}R_2}{g_{m9}R_{ds14}} \Delta V_{DD}
$$

(4.20)

$$
= \left(1 - \frac{g_{mi}R_1}{g_{m9}R_{ds14}}\right) g_{m2}R_2\Delta V_{DD}
$$

Finally, regarding path 5, there are two ways for the supply noise injecting into output. The first way is due to the non-zero $V_{GS}$ of $M_P$. The second way is due to the limited $R_{dsP}$ of $M_P$. Based on (4.20), the noise at the output can be derived as

$$
\Delta V_{OUT} = g_{mp}z_{out\_reg} \left[1 - \left(1 - \frac{g_{mi}R_1}{g_{m9}R_{ds14}}\right) g_{m2}R_2\right] \Delta V_{DD} + \frac{z_{out\_reg}}{z_{out\_reg} + R_{dsP}} \Delta V_{DD}
$$

(4.21)
As such, the PSR of the LDO regulator at low frequency can be expressed

\[
PSR = g_{mp}\frac{z_{out\_reg}}{z_{out\_reg} + R_{d}} \left[ 1 - \left( 1 - \frac{g_m R}{g_m R_{d14}} \right) g_m R_2 \right] + \frac{z_{out\_reg}}{z_{out\_reg} + R_{d}} \left[ 1 - \left( 1 - \frac{g_m R}{g_m R_{d14}} \right) g_m R_2 \right]
\]

\[
\approx g_{mp} \frac{(1 + s/p_{-3dB})(1 + s)(1/g_m)R_{d}}{A_{dc} R_{d} - \left[ 1 - \left( 1 - \frac{g_m R}{g_m R_{d14}} \right) g_m R_2 \right] + \frac{1}{R_{d}}}
\]

(4.22)

From (4.22), it can be seen that a good PSR can be achieved at low frequency by control the design parameters of \(g_{m1}, g_{m2}, g_{m9},\) and \(A_{dc} \). In addition, when frequency is larger than \(p_{-3dB}\), the PSR will starts to drop as the loop gain starts to drop when frequency increases.

(ii) At moderate frequency, the loop gain of the LDO regulator equals or smaller than 1. The Miller compensation capacitor shorts the gate and drain nodes of \(M_D\), forcing it to work as a diode transistor. As a result, the supply noise will directly inject to node \(N_1\) through \(M_D\) and couple to \(V_{OUT}\) through \(C_{m1}\). The PSR for this range is around 0 dB.

(iii) At high frequency, capacitor \(C_L\) shorts the output to ground, the PSR of the LDO regulator becomes smaller when frequency increases.

Figure 4.8 depicts the simulated PSR of LDO regulator under \(I_L = 50 \text{ mA}\) for \(C_L = 10 \text{ pF}, 100 \text{ pF}, 1 \text{ nF}\) and \(10 \text{ nF}\), respectively. It can be seen that the PSR of LDO regulator follows the theoretical prediction and validates the analysis above: (i) At low frequency, the PSR of the regulator is determined by the feedback loop gain and shows a zero at \(p_{-3dB}\). (ii) At moderate frequency, the PSR of the LDO regulator is around 0 dB. (iii) At high frequency, the PSR becomes smaller due to the output capacitor
filtering effect. For a large capacitor, the filtering effect will be stronger and the PSR will reduce at a lower frequency as indicated in Fig. 4.8.

Fig. 4.8 Simulated PSR of the LDO regulator under $I_L = 50$ mA for different $C_L$. 
4.4. Simulation Results and Performance Comparison

This Section presents the simulation results together with discussions. The performance comparison with the reported state-of-the-art OCL-LDO regulators is also investigated.

4.4.1. Simulation Results and Discussions

The proposed FVF LDO regulator using DSMFC technique is realized in a UMC 65-nm CMOS process. The compensation capacitors $C_{m1}$ and $C_{m2}$ are each in 4 pF. It consumes a quiescent current of 23.7 $\mu$A at typical process and room temperature with 1.2 V voltage supply. The LDO regulator provides a 1 V output voltage with a maximum of 50 mA $I_L$. More importantly, it is able to drive a $C_L$ range of 10 pF – 10 nF with good transient response. Figure 4.9 shows the transient responses for the LDO regulator with full current step (0 to 50 mA) at four different $C_L$ values. When $I_L$ switches between 0 and 50 mA with a 100 ns edge time, the undershoots are 41 mV, 40 mV, 46 mV and 58 mV whereas the overshoots are all close to 19 mV for $C_L = 10$ pF, 100 pF, 1 nF and 10 nF, respectively.
To demonstrate the robustness of the proposed design, Table 4.6 lists the PM and GM, quiescent current ($I_Q$), load regulation, power supply rejection (PSR) and the load transient responses of the LDO regulator under extreme temperatures and process corners. Except the PM and GM, all the other parameters are obtained with $C_L = 100\, \text{pF}$. The PM and GM are simulated across the whole $C_L$ range and $I_L$ range. The minimum values or worst case values are obtained and presented in Table 4.6. For the load transient responses, two different load current switching steps (0 to 50 mA, and 1 mA to 50 mA) are used.

From Table 4.6, it can be concluded that the proposed LDO regulator is stable even under process and temperature variations with sufficient PM (> 45°) and GM (> 6 dB).
Moreover, the LDO regulator’s transient performance does not change significantly for different corners, especially when \( I_L \) switches between 1 mA to 50 mA.

### 4.4.2. Performance Comparison

Performance comparison between the proposed LDO regulator with other reported OCL-LDO regulators is presented in Table 4.7. To compare the \( C_L \) driving ability and the frequency compensation efficiency, the maximum \( C_L \) to the total compensation capacitance ratio \( (C_{L,\text{max}}/C_C) \) is introduced. As indicated in Table 4.7, with the DSMFC technique, the proposed LDO regulator achieves the widest \( C_L \) range and the highest \( C_{L,\text{max}}/C_C \) ratio.

To compare the load transient performance, the OCL-LDO regulator figure-of-merit (FOM) [24] is adopted. It is given by

\[
\text{FOM} = \frac{V_{\text{OUT,typ}}}{I_L} = \frac{\Delta V_{\text{OUT,U1}} + \Delta V_{\text{OUT,O1}} + \Delta V_{\text{OUT,U2}} + \Delta V_{\text{OUT,O2}}}{I_L}
\]

\[
\Delta V_{\text{OUT,U1}}, \Delta V_{\text{OUT,O1}}, T_{\text{SETTLE1}}, \Delta V_{\text{OUT,U2}}, \Delta V_{\text{OUT,O2}}, T_{\text{SETTLE2}} \text{ represent the undershoot, overshoot and settling time for } I_L \text{ switching from 0-50 mA and 1-50 mA, respectively.}

### Table 4.6 Performance Summary under Process and Temperature Corners

<table>
<thead>
<tr>
<th>Parameter</th>
<th>27 °C</th>
<th>-40 °C</th>
<th>90 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corner</td>
<td>TT</td>
<td>SS</td>
<td>SF</td>
</tr>
<tr>
<td>( PM_{\text{min}} ) (degree)</td>
<td>50.4</td>
<td>50.9</td>
<td>55.4</td>
</tr>
<tr>
<td>( GM_{\text{min}} ) (dB)</td>
<td>7.8</td>
<td>6.1</td>
<td>6.9</td>
</tr>
<tr>
<td>( I_Q ) (μA)</td>
<td>23.7</td>
<td>14.1</td>
<td>18.1</td>
</tr>
<tr>
<td>Load Reg. (μV/mA)</td>
<td>34</td>
<td>24</td>
<td>22</td>
</tr>
<tr>
<td>PSR (dB)</td>
<td>-52</td>
<td>-47.6</td>
<td>-53</td>
</tr>
<tr>
<td>( \Delta V_{\text{OUT,U1}} ) (mV)</td>
<td>40</td>
<td>34.1</td>
<td>35.7</td>
</tr>
<tr>
<td>( \Delta V_{\text{OUT,O1}} ) (mV)</td>
<td>18.1</td>
<td>20.4</td>
<td>17.5</td>
</tr>
<tr>
<td>( T_{\text{SETTLE1}} ) (μs)</td>
<td>1.65</td>
<td>1.27</td>
<td>1.31</td>
</tr>
<tr>
<td>( \Delta V_{\text{OUT,U2}} ) (mV)</td>
<td>25.7</td>
<td>24.4</td>
<td>21.2</td>
</tr>
<tr>
<td>( \Delta V_{\text{OUT,O2}} ) (mV)</td>
<td>18.2</td>
<td>20.1</td>
<td>16.2</td>
</tr>
<tr>
<td>( T_{\text{SETTLE2}} ) (μs)</td>
<td>0.94</td>
<td>0.79</td>
<td>0.66</td>
</tr>
</tbody>
</table>


\( \Delta V_{\text{OUT,U1}}, \Delta V_{\text{OUT,O1}}, T_{\text{SETTLE1}}, \Delta V_{\text{OUT,U2}}, \Delta V_{\text{OUT,O2}}, T_{\text{SETTLE2}} \) represent the undershoot, overshoot and settling time for \( I_L \) switching from 0-50 mA and 1-50 mA, respectively.
\[ FOM = K \left( \frac{\Delta V_{\text{OUT}} \times I_Q}{\Delta I_{\text{OUT}}} \right) \]  

(4.23)

where \( K \) is the edge time ratio defined as

\[
K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among the designs for comparison}}
\]

(4.24)

In Table 4.7, the smallest edge time (100 ps in [18]) is used as the reference while the others are normalized values. To get a fair comparison, all the parameters of the proposed LDO regulator is simulated at \( C_L = 100 \text{ pF} \). Furthermore, some of the LDO regulators [23, 24] were tested with some amount of minimum \( I_L \). Therefore, two FOMs are obtained for the proposed FVF LDO regulator. The first one utilizes a \( I_L \) switching from 0 to 50 mA and vice versa, and the second one is based on the \( I_L \) switches between 1 mA to 50 mA. From Table 4.7, it can be observed that the proposed LDO regulator achieves a comparable or better FOM when compared with those of reported OCL-LDO regulators. It also gives reasonable and good results for other performances like load regulation, line regulation, settling time and PSR.

Comparing with the original LDO regulator [34] with wide load capacitance range driving capability, the proposed topology displays better transient performance due to a smaller power transistor, a simple non-inverting gain stage, smaller compensation capacitors and an increased quiescent power.
### Table 4.7 Performance Comparison with the Reported OCL-LDO Regulators

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[18]</th>
<th>[21]</th>
<th>[22]</th>
<th>[23]</th>
<th>[24]</th>
<th>[26]</th>
<th>[27]</th>
<th>[30]</th>
<th>[34]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology (μm)</td>
<td>0.09</td>
<td>0.35</td>
<td>0.35</td>
<td>0.35</td>
<td>0.09</td>
<td>0.35</td>
<td>0.35</td>
<td>0.065</td>
<td>0.065</td>
<td>0.065</td>
</tr>
<tr>
<td>(V_{\text{IN}}) (V)</td>
<td>1.2</td>
<td>3</td>
<td>1.2-1.5</td>
<td>0.95-1.4</td>
<td>0.75-1.2</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>(V_{\text{OUT}}) (V)</td>
<td>0.9</td>
<td>2.8</td>
<td>1</td>
<td>0.7-1.2</td>
<td>0.5-1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Dropout Voltage (mV)</td>
<td>300</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>(I_{\text{Q}}) (μA)</td>
<td>600</td>
<td>65</td>
<td>95</td>
<td>43</td>
<td>8</td>
<td>408</td>
<td>28</td>
<td>0.9</td>
<td>13.2</td>
<td>23.7*</td>
</tr>
<tr>
<td>(I_{\text{OUT}}) (max) (mA)</td>
<td>100</td>
<td>50</td>
<td>50</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Total On-Chip Cap. ((C_{\text{T}}), pF)</td>
<td>600</td>
<td>21</td>
<td>0</td>
<td>6</td>
<td>7</td>
<td>1.8</td>
<td>10</td>
<td>4.5</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>Total Comp. Cap. ((C_{\text{C}}), pF)</td>
<td>N/A</td>
<td>21</td>
<td>N/A</td>
<td>N/A</td>
<td>1.6</td>
<td>1.5</td>
<td>10</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load Cap. Range ((C_{\text{L}}, F))</td>
<td>N/A</td>
<td>0-100p</td>
<td>N/A</td>
<td>0, 100p, 1n</td>
<td>0-50p</td>
<td>0-1n</td>
<td>0-100p</td>
<td>0-100p</td>
<td>10p-10n</td>
<td>10p-10n*</td>
</tr>
<tr>
<td>Line Reg. (mV/V)</td>
<td>N/A</td>
<td>23</td>
<td>18</td>
<td>N/A</td>
<td>3.78</td>
<td>4.3</td>
<td>0.39</td>
<td>4.7</td>
<td>217</td>
<td>8.89</td>
</tr>
<tr>
<td>Load Reg. (μV/mA)</td>
<td>1800</td>
<td>560</td>
<td>280</td>
<td>400</td>
<td>100</td>
<td>3</td>
<td>78.2</td>
<td>300</td>
<td>133</td>
<td>34</td>
</tr>
<tr>
<td>PSR @1kHz, (I_{\text{L}} = 50\text{mA}) (dB)</td>
<td>N/A</td>
<td>-57</td>
<td>N/A</td>
<td>N/A</td>
<td>-44</td>
<td>-56</td>
<td>-49.8</td>
<td>N/A</td>
<td>N/A</td>
<td>-52</td>
</tr>
<tr>
<td>(T_{\text{SETTLE}}) (μs)</td>
<td>N/A</td>
<td>15</td>
<td>0.3</td>
<td>3</td>
<td>5</td>
<td>N/A</td>
<td>N/A</td>
<td>6</td>
<td>0.925</td>
<td>1.65</td>
</tr>
<tr>
<td>(\Delta V_{\text{OUT}}) (mV)</td>
<td>90</td>
<td>90</td>
<td>N/A</td>
<td>70</td>
<td>114</td>
<td>35</td>
<td>105</td>
<td>68.8</td>
<td>341.6</td>
<td>40</td>
</tr>
<tr>
<td>(\Delta I_{\text{OUT}}) (mA)</td>
<td>100</td>
<td>50</td>
<td>50</td>
<td>99</td>
<td>97</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Edge Time (μs)</td>
<td>0.0001</td>
<td>1</td>
<td>0.5</td>
<td>1</td>
<td>0.1</td>
<td>0.01</td>
<td>1</td>
<td>0.3</td>
<td>0.5</td>
<td>0.1*</td>
</tr>
<tr>
<td>Edge Time Ratio K</td>
<td>1</td>
<td>10000</td>
<td>5000</td>
<td>10000</td>
<td>1000</td>
<td>10000</td>
<td>10000</td>
<td>3000</td>
<td>5000</td>
<td>1000</td>
</tr>
<tr>
<td>FOM</td>
<td>0.0054</td>
<td>1.17</td>
<td>0.304</td>
<td>0.0094</td>
<td>0.014</td>
<td>0.294</td>
<td>0.0019</td>
<td>0.45</td>
<td>0.019</td>
<td>0.012</td>
</tr>
<tr>
<td>(C_{\text{L(max)}}/C_{\text{C}})</td>
<td>N/A</td>
<td>4.76</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>625</td>
<td>11.11</td>
<td>66.67</td>
<td>1000</td>
<td>1250</td>
</tr>
</tbody>
</table>

# The quiescent current includes the current consumptions of the biasing circuit and the OTA control voltage generator.
† Load capacitance range under worst process and temperature variations.
* Transient performance for \(I_{\text{L}}\) switches between 1 mA and 50 mA.
4.5. Summary

Due to the large parasitic capacitance at the supply line of the digital circuit, the LDO regulator need support wide load capacitance range with good transient performance metrics. In this Chapter, a FVF based LDO regulator with Dual-Summed Miller Frequency Compensation (DSMFC) is presented. Implemented with a simple resistive-loaded inverting amplifier, the DSMFC not only forms the low frequency dominant pole together with the conventional Miller compensation, it also shifts the non-dominant pole(s) to a higher frequency, especially under low and moderate load currents. The detailed stability analysis and simulation investigations have demonstrated that the proposed LDO regulator topology can support wide load capacitance range (10 pF to 10 nF) for different load current conditions whilst maintaining very good transient performance. It reaches a comparable or better FOM and achieves the highest $C_{L(max)}/C_C$ ratio with respect to other reported OCL-LDO regulator topologies. Therefore, it is useful for wide load capacitance range applications.
CHAPTER 5

WIDE LOAD CAPACITANCE RANGE OCL-LDO REGULATOR: TYPE-II

In this Chapter, the Type-II wide $C_L$ range OCL-LDO regulator is discussed. The proposed topology and its working principle, stability analysis, design strategy, circuit implementation and simulation and measurement results are all explored in detail.

5.1. Proposed Negative Current Feedback Technique

As discussed in Chapter 3, to achieve a fast-transient LDO regulator, the charging/discharging at the gate of power transistor must be high. Meanwhile, the loop gain of the regulator must be high enough to ensure good regulation accuracy. Therefore, another fast transient multi-gain stage regulator topology is shown in Fig. 5.1. Similar to the definitions in Chapter 3, $g_{mi}$ denotes the transconductance while $R_i$ and $C_i$ are the equivalent output resistance and lumped output parasitic capacitance of the $i$-th gain stage, respectively. $R_O$ is the effective output resistance which includes the output resistance of power transistor as well as the loading resistance $R_L$.

![Fig. 5.1](image_url)

Fig. 5.1: A fast-transient multi-gain stage regulator topology.
In this topology, $R_2$ is designed to be high whereas $R_P$ is designed to be dominantly small ($\approx 1/g_m$). With this implementation, the $3^{\text{rd}}$ gain stage can be dynamically biased which will increase the charging/discharging rate of $V_P$. As a result, the speed of the regulator is greatly improved with respect to the conventional topology (Fig. 3.3). It is important to note that $C_P$ and $R_3$ may be large. They lead to large $C_P R_P$ and $C_2 R_2$, respectively. Based on Routh–Hurwitz stability criterion, the large time constant $C_2 R_2$ and $C_P R_P$ may introduce a right-half-plane (RHP) pole. To address this issue, a negative current feedback (NCF) technique is employed to avoid the RHP pole formation which is shown in Fig. 5.2.

![Fig. 5.2: Proposed Negative Current Feedback (NCF) topology embedded in multi-gain stage in a LDO regulator.]

In the NCF block depicted in Fig. 5.2, the current sensor senses the voltage $V_P$ and generates a transconductance current $g_{mf} V_P$ ($g_{mf}$ is the transconductance of the current sensor). The generated current is then fed back to the node $N_2$. Not only does the feedback current increase the biasing current of $2^{\text{nd}}$ stage as the first effect, it also forms a local negative current feedback loop (NCF loop in Fig. 5.2) as the second effect. Combining these two effects, the output impedance at node $N_2$ is reduced from $R_2$ to $R_{2f}$ ($R_{2f}$ is the negative current feedback loaded impedance at node $N_2$). As such,
both $C_2R_{2f}$ and the regulator loop gain are reduced. This permits the feedback system to fulfill the Routh–Hurwitz stability criterion without introducing RHP pole. In addition, the NCF technique adds another advantage by shifting the non-dominant poles to a higher frequency. Hence the stability of the LDO regulator can be attained in the context of wide range of capacitive load ($C_L$) and load current ($I_L$).

However, there are two tradeoff issues in the design of NCF LDO regulator. They are given as follows: (i) The gain of 2$^{nd}$ stage is reduced because of a smaller $R_{2f}$. This in turn reduces the total loop gain of the LDO regulator, thus sacrificing some regulation accuracy. (ii) The negative feedback current reduces the charging/discharging rate of the node $N_2$, which can reduce the transient speed. In view of the two drawbacks, a weighted current feedback (WCF) circuit technique [96] is further proposed to tackle the limitations arising from the foundation NCF technique.
5.2. Proposed Weighted Current Feedback Technique

Figure 5.3 shows a LDO regulator architecture using the WCF circuit technique. It comprises a fixed first gain stage, two variable gain stages (2\textsuperscript{nd} and 3\textsuperscript{rd} gain stages), a WCF block, a power transistor $M_p$, an overshoot reduction block and a frequency compensation network.

The shadowed area embodies the 2\textsuperscript{nd}, 3\textsuperscript{rd} gain stages as well as the WCF circuit (dash enclosed box). In the WCF circuit, two sense transistors ($M_{a1}$ and $M_{a2}$; size of $M_{a2}$ > size of $M_{a1}$) sense the same voltage $V_p$ and each generates respective feedback current ($I_{a1}$, $I_{a2}$) at the output of 2\textsuperscript{nd} gain stage. Moreover, the diode transistor $M_{a3}$ is added in series with $M_{a4}$ to control the operating region of $M_{a2}$ during the change of $I_L$.

The working principle of the WCF technique can be explained from Fig. 5.4. (i) At low $I_L$ (Fig. 5.4(a)), both $M_{a1}$ and $M_{a2}$ are weakly biased for small negative current feedback. Each 2\textsuperscript{nd} and 3\textsuperscript{rd} gain stage works as a normal inverting amplifier. (ii) At moderated $I_L$ (Fig. 5.4(b)), both $M_{a1}$ and $M_{a2}$ are designed to work in saturation region. Two feedback currents ($I_{a1}$, $I_{a2}$ and $I_{a2} > I_{a1}$) are generated and fed back to the node $N_2$. This results in a strong negative current feedback to the 2\textsuperscript{nd} stage. (iii) At high $I_L$ (Fig. 5.4(c)), only $M_{a1}$ works in saturation region to give a small negative current feedback. $M_{a2}$ is forced to work in linear region by the two diode transistors, $M_{a3}$ and $M_{a4}$. Hence, the negative current feedback is reduced. Owing to this weighted control mechanism in the WCF technique, the impedance at the node $N_2$ as well as the gain of 2\textsuperscript{nd} stage can be dynamically managed. Therefore, with reference to the proposed NCF technique, the advantages are as follows: (i) The gain of the WCF LDO regulator can be maintained reasonably well across the whole $I_L$ range such that better regulation accuracy can be achieved. (ii) The charging/discharging rate of node $N_2$ is increased at high $I_L$, which results in faster transient speed.
Fig. 5.3: A LDO regulator architecture using the WCF technique.
Fig. 5.4: Simplified schematic of 2nd, 3rd gain stages and WCF for (a) low $I_L$, (b) moderate $I_L$, and (c) high $I_L$. 
The 3\textsuperscript{rd} gain stage is loaded by a resistor $R_X$ and a diode transistor $M_{d1}$. The output impedance of this gain stage ($R_p \approx (1/g_{md1})//R_X$, $g_{md1}$ representing the transconductance of $M_{d1}$) reduces when $I_L$ increases. In this way, the resistor and diode transistor load provides an adaptive bias when $I_L$ changes. This subsequently increases the speed of 3\textsuperscript{rd} gain stage.

Turning to the frequency compensation design, a combined frequency compensation scheme using both cascode and Miller compensation techniques is adopted. The dominant pole is mainly formed by the cascode compensation capacitor whilst a small Miller compensation capacitor is utilized to reduce the Q factor of complex poles.

To complete the LDO architecture, an overshoot reduction block [30] is employed to reduce the overshoot magnitude and the settling time through a momentary discharging current.
5.3. Dynamic Impedance Reduction and Small-Signal Model for WCF LDO Regulator

To investigate the negative current feedback loaded impedance $R_{2f}$ at the node $N_2$, the small-signal model of the WCF LDO regulator is depicted in Fig. 5.5. It is obtained by breaking the loop at the output node as shown in Fig. 5.3. In the small-signal model, $g_{mi}$, $R_i$, and $C_i$ have their usual meanings as defined in Section 5.1. Particularly, $C_c$ is the cascode compensation capacitor whereas $C_m$ is the Miller compensation capacitor. $C_L$ is the load capacitance which has a value ranging from 470 pF to 10 nF.

![Small-signal model of the WCF LDO regulator.](image)

Refer to Fig. 5.5, the total gain of the WCF feedback loop ($A_{WCF}$) in Fig. 5.3 is examined. It is given as

$$A_{WCF} = g_{m3}g_{mf}R_2R_P$$  \hspace{1cm} (5.1)

while $R_{2f}$ can be obtained as

$$R_{2f} = \frac{R_2}{A_{WCF} + 1} = \frac{R_2}{\beta g_{m3}g_{mf} R_P + \frac{1}{R_2}}$$  \hspace{1cm} (5.2)

Comparing to the output impedance $R_2$ (without loaded feedback current source) in
R_{2f} is reduced by \( \beta \) (= A_{WCF} + 1) times. In addition, R_{2f} can be reduced via either increasing A_{WCF} or decreasing R_2. Using this relationship in the WCF LDO regulator, at low I_L, R_{2f} is large since \( \beta \) is small and R_2 is large. At moderate I_L, R_{2f} is significantly reduced with respect to R_2 due to a large \( \beta \). At high I_L, since R_2 is already small owing to a large current flowing in the 2\textsuperscript{nd} gain stage, R_{2f} is small even with a small \( \beta \).

As for the transfer function of the whole WCF LDO regulator, it is derived using the following assumptions: (i) \( C_1, C_2 \ll C_m \ll C_c \ll C_L \); (ii) \( g_m R_1, g_m R_2 \gg 1 \), (iii) the input resistance at the cascode compensation node, is approximately equal to \( 1/g_{mc} \) and (iv) \( R_P \) is inversely proportional to I_L. Finally, the open-loop transfer function is obtained as follows:

\[
A_{op}(s) = \frac{v_{fbout}}{v_{bin}} = -\frac{A_{DC} \left(1 + s \frac{C_c}{g_{mc}}\right)}{1 + a s + b s^2 + c s^3 + d s^4 + e s^5} \quad (5.3)
\]

where

\[
a = C_L R_O + C_c g_{m2} g_{m3} R_1 R_2 R_P R_O / \beta \quad (5.4)
\]

\[
b = C_m C_L R_1 R_O + C_c C_m g_{m2} g_{m3} R_1 R_2 R_P R_O / (\beta g_{mc}) \quad (5.5)
\]

\[
c = C_m C_L R_1 R_O (C_c / g_{mc} + C_P R_P / \beta) \quad (5.6)
\]

\[
d = C_c C_m C_L C_c R_1 R_P R_O / (\beta g_{mc}) \quad (5.7)
\]

\[
e = C_c C_m C_L C_c R_1 R_2 R_P R_O / (\beta g_{mc}) \quad (5.8)
\]

The DC loop gain of the LDO regulator is given by

\[
A_{DC} = g_m g_{m2} g_{m3} R_1 R_2 R_P R_O / \beta \quad (5.9)
\]
which indicates that the loop gain is reduced by a factor of $\beta$. This correlates well with the impedance reduction at the node $N_2$, namely, $R_{2f} = R_2/\beta$. Besides, the cascode compensation generates a zero which is expressed as

$$z = -\frac{g_{mc}}{C_c}$$  \hspace{1cm} (5.10)

Using (5.3) – (5.10), the stability of LDO regulator can be analyzed.
5.4. Stability Analysis and WCF Design Strategy

This section presents the stability and WCF design strategy of the WCF LDO regulator. The design strategy of the WCF technique is on the basis of the stability of the LDO regulator at different $C_L$ and $I_L$ conditions. Firstly, using the Routh–Hurwitz stability criterion, the required $\beta$ (denoted as $\beta_{RH}$) can be obtained. Secondly, under a PM of $45^\circ$ constraint, the required $\beta$ (denoted as $\beta_{PM}$) is also investigated. The respective analysis is explained in the following.

As indicated in (5.4) to (5.8), all the parameters in the transfer function are a function of $C_L R_O$. Moreover, $C_L$ varies from 470 pF to 10 nF and $R_O$ is inversely proportional to $I_L$. For this reason, the design strategy for $\beta$ and the stability of the regulator are analyzed in three cases: (I) $C_L R_O$ is large (low $I_L$). The first term in (5.4) and (5.5) are dominant. (II) $C_L R_O$ is moderate (low $I_L$). The first term is comparable with second term in (5.4) and the first term in (5.5) is dominant. (III) $C_L R_O$ is small (moderate $I_L$ and high $I_L$). The second term in (5.4) and (5.5) are dominant. Besides, the term $C_p R_p/\beta$ in (5.6) is small due to a small $R_p$. Finally, the respective simplified expression for variables from a to e is summarized in Table 5.1.
5.4.1. Design Strategy of $\beta$ using Routh–Hurwitz Stability Criterion

Routh–Hurwitz stability criterion has been widely used in the multi-stage amplifier designs [97-99]. It is simply evaluated by constructing the Routh Table 5.2 using the closed-loop transfer function. To achieve stability for the feedback system, the coefficients for $a_0$–$a_5$ and $b_1$, $c_1$, $d_1$ in the second column of Table 5.2 must be positive. Since $a_0$–$a_5$ is always larger than zero, the design condition for $\beta_{RH}$ can be obtained by setting $b_1$, $c_1$ and $d_1$ larger than zero respectively.

### Table 5.1 Approximated Variables from a to e For Large, Moderate and Small $C_LR_O$ Cases

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Large $C_LR_O$</th>
<th>Moderate $C_LR_O$</th>
<th>Small $C_LR_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>a</strong></td>
<td>$(5.4)$ $C_LR_O$</td>
<td>$2C_LR_O$</td>
<td>$C_cg_{m2}g_{m3}g_{mp}R_1R_2R_3R_0/\beta$</td>
</tr>
<tr>
<td><strong>b</strong></td>
<td>$(5.5)$ $C_mC_LR_1R_0$</td>
<td>$C_mC_cg_{m2}g_{m3}g_{mp}R_1R_2R_3R_0/\beta g_{mc}$</td>
<td></td>
</tr>
<tr>
<td><strong>c</strong></td>
<td>$(5.6)$ $C_mC_LR_1R_0(C_c/g_{mc} + C_pR_p/\beta)$</td>
<td>$C_mC_cC_pR_R_O/g_{mc}$</td>
<td></td>
</tr>
<tr>
<td><strong>d</strong></td>
<td>$(5.7)$ $C_cC_mC_pC_LR_1R_2R_3R_0(\beta g_{mc})$</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>e</strong></td>
<td>$(5.8)$ $C_cC_mC_pC_LR_1R_2R_3R_0(\beta g_{mc})$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 5.2 Routh Table for a 5th Order Polynomial

<table>
<thead>
<tr>
<th>$s^5$</th>
<th>$a_5$</th>
<th>$a_4$</th>
<th>$a_3$</th>
<th>$a_2$</th>
<th>$a_1$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$s^4$</td>
<td>$a_4$</td>
<td>$a_3$</td>
<td>$a_2$</td>
<td>$a_1$</td>
<td></td>
</tr>
<tr>
<td>$s^3$</td>
<td>$b_1 = (a_3a_4 - a_2a_5)/a_4$</td>
<td>$b_2 = (a_4a_5 - a_3a_2)/a_4$</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$s^2$</td>
<td>$c_1 = (a_2b_1 - a_1b_2)/b_1$</td>
<td>$c_2 = a_0$</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$s^1$</td>
<td>$d_1 = (b_2c_1 - a_0b_1)/c_1$</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$s^0$</td>
<td>$e_1 = a_0$</td>
<td>0</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Refer to the WCF LDO regulator, the closed-loop transfer function can be expressed as

\[
A_{cl}(s) = \frac{A_{op}(s)}{1 - A_{op}(s)} \approx \frac{-A_{DC}(1 + sC_c/g_{mc})}{A_{DC} + (A_{DC}C_c/g_{mc} + a)s + bs^2 + cs^3 + ds^4 + es^5}
\]  \hspace{1cm} (5.11)

where \(A_{op}(s)\) is the open-loop transfer function defined in (5.3). By substituting the approximated expression for variables a to e from Table 5.1 as well as (5.9)–(5.10) into (5.11), the Routh table parameter expansion for Large, Moderate and Small \(C_{L}R_{O}\) cases is listed in Table 5.3. Based on these parameters, \(\beta_{RH}\) for each case is analyzed as follows:

**Case I:** Large \(C_{L}R_{O}\) (Low \(I_{L}\)) condition, the Routh Table parameters are shown in Case I of Table 5.3. To meet the stability criterion, the following conditions must be satisfied. They are obtained as

\[
C_mC_LR_{O}(C_c/g_{mc} + C_pR_p/\beta_{RH}) > 0
\]  \hspace{1cm} (5.12)

\[
C_mC_LR_{O} > 0
\]  \hspace{1cm} (5.13)

\[
\beta_{RH} > C_cg_{m}g_{m2}g_{m3}g_{mp}R_{R2}R_{P}/(C_c/g_{mc})
\]  \hspace{1cm} (5.14)

For (5.12) and (5.13), it is obviously valid for any \(\beta_{RH}\). As for (5.14), the right hand side term is inversely proportional to \(C_L\). Since \(C_L\) ranges from 470 pF to 10 nF, \(\beta_{RH}\) is small in this case.

**Case II:** Moderate \(C_{L}R_{O}\) (Low \(I_{L}\)) condition, when \(C_{L}R_{O}\) is equal to the cascode compensation term, namely,

\[
C_cg_{m2}g_{m3}g_{mp}R_{R2}R_{P}/\beta = C_LR_{O}
\]  \hspace{1cm} (5.15)
### Table 5.3 Routh Table Parameter Expansion for the WCF LDO Regulator Closed-Loop Transfer Function in (5.11)

<table>
<thead>
<tr>
<th>Par.</th>
<th>Case I (Large $C_L R_o$)</th>
<th>Case II (Moderate $C_L R_o$)</th>
<th>Case III (Small $C_L R_o$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_0$</td>
<td>$g_{m1}g_{m2}g_{m3}g_{mp}R_{R_1}R_{R_2}R_{R_3}/\beta$</td>
<td>$g_{m1}g_{m2}g_{m3}g_{mp}R_{R_1}R_{R_2}R_{R_3}/\beta$</td>
<td>$g_{m1}g_{m2}g_{m3}g_{mp}R_{R_1}R_{R_2}R_{R_3}/\beta$</td>
</tr>
<tr>
<td>$a_1$</td>
<td>$C_L R_o$</td>
<td>$(2 + g_{m1}/g_{mc}) C_L R_o$</td>
<td>$(1 + g_{m1}/g_{mc}) C_L R_o$</td>
</tr>
<tr>
<td>$a_2$</td>
<td>$C_m C_L R_1 R_o$</td>
<td>$C_m C_L R_1 R_o$</td>
<td>$C_m C_L R_1 R_o / (\beta g_{mc})$</td>
</tr>
<tr>
<td>$a_3$</td>
<td>$C_m C_L R_1 R_o (C_c / g_{mc} + C_p R_p / \beta)$</td>
<td>$C_c C_m C_L R_1 R_o / g_{mc}$</td>
<td>$C_c C_m C_L R_1 R_o / (\beta g_{mc})$</td>
</tr>
<tr>
<td>$a_4$</td>
<td>$C_c C_m C_p C_L R_1 R_o R_p / (\beta g_{mc})$</td>
<td>$C_c C_m C_p C_L R_1 R_o R_p / (\beta g_{mc})$</td>
<td></td>
</tr>
<tr>
<td>$a_5$</td>
<td>$C_c C_m C_p C_L R_1 R_o R_p / (\beta g_{mc})$</td>
<td>$C_c C_m C_p C_L R_1 R_o R_p / (\beta g_{mc})$</td>
<td></td>
</tr>
<tr>
<td>$b_1$</td>
<td>$C_m C_L R_1 R_o (C_c / g_{mc} + C_p R_p / \beta)$</td>
<td>$(C_L - C_p g_{m2}g_{m3}g_{mp}R_p^2 / \beta) C_m R_o / g_{mc}$</td>
<td>$(C_x - C_p g_{m1}g_{mc}g_{mp}R_p^2 / \beta) C_m R_o / g_{mc}$</td>
</tr>
<tr>
<td>$b_2$</td>
<td>$C_L R_o$</td>
<td>$(2 + g_{m1}/g_{mc}) C_L R_o$</td>
<td>$(1 + g_{m1}/g_{mc}) C_m g_{m2}g_{m3}g_{mp}R_{R_2}R_{R_3}/\beta$</td>
</tr>
<tr>
<td>$c_1$</td>
<td>$C_m C_L R_1 R_o$</td>
<td>$[\chi C_m / g_{mc} - (1 + g_{m1}/g_{mc}) C_p C_L R_p / \beta] C_m R_o / g_{mc}$</td>
<td>$[\chi C_m / g_{mc} - (1 + g_{m1}/g_{mc}) C_p C_L R_p / \beta] C_m R_o / g_{mc}$</td>
</tr>
<tr>
<td>$c_2$</td>
<td>$a_0$</td>
<td>$a_0$</td>
<td></td>
</tr>
<tr>
<td>$d_1$</td>
<td>$C_L R_o - C_c g_{m1}g_{m2}g_{m3}g_{mp}R_{R_2}R_{R_3}/\beta g_{mc}$</td>
<td>$C_L R_o \left[ 2 - C_p R_p g_{m1}/\beta C_c \right]$</td>
<td>$C_L R_o \left[ 2 - C_p R_p g_{m1}/\beta C_c \right]$</td>
</tr>
</tbody>
</table>

* $\chi = C_L - C_p g_{m2}g_{m3}g_{mp}R_p^2 / \beta$
the Routh Table parameters are shown in Case II of Table 5.3. As indicated, \( b_1 \) and \( c_1 \) for Case I and Case II are the same. The design conditions for \( b_1 > 0 \) and \( c_1 > 0 \) can still be expressed by (5.12) and (5.13), respectively. Since (5.12) and (5.13) are always valid for any \( \beta_{RH} \), the condition for \( \beta_{RH} \) to meet the criterion is obtained as

\[
\beta_{RH} > C_P g_{m1} R_P/(2C_c)
\]  

(5.16)

From (5.16), the right hand side term is proportional to \( g_{m1} R_P \). Since the maximum value for \( R_P \) is \( R_X \) as explained in Section 5.2, \( \beta_{RH} \) can be made small by proper sizing of \( R_P \) and \( g_{m1} \).

**Case III:** Small \( C_L R_O \) (Moderate and High \( I_L \)) condition, the Routh Table parameters are shown in Case III of Table 5.3. To meet the criterion, the following three design requirements for \( \beta_{RH} \) must be fulfilled. They are expressed as

\[
\beta_{RH} > C_2 g_{m2} g_{m3} g_{mp} R_2^2 R_P/C_L
\]  

(5.17)

\[
\beta_{RH} > (1 + g_{m1}/g_{mc}) C_P g_{mc} R_P/C_m
\]  

(5.18)

\[
\beta_{RH} > C_2 g_{m2} g_{m3} g_{mp} R_2^2 R_P/C_L + \left(1 + g_{m1}/g_{mc}\right) C_P g_{mc} R_P/C_m
\]  

(5.19)

If the condition in (5.19) is met, (5.17) and (5.18) will be valid as well, but not vice versa. This suggests that (5.19) determines the only choice out of three \( \beta_{RH} \) inequalities. As such, at moderate \( I_L \), \( R_2 \) and \( R_P \) are fairly large. \( \beta_{RH} \) is the largest. On the other hand, at high \( I_L \), \( R_P \) is small owing to the large biasing current flowing in the diode transistor \( M_{d1} \) of 3rd gain stage. \( R_2 \) is also small due to the dynamic bias introduced by the WCF block. Thus \( \beta_{RH} \) at high \( I_L \) condition is reduced with respect to that of moderate \( I_L \) case. Based on the above analysis, Table 5.4 summarizes the \( \beta_{RH} \) at different \( I_L \).
conditions. From this table, it confirms that the WCF should be made strong at moderate $I_L$ condition whilst weak at both low and high $I_L$ conditions.

### Table 5.4 Summary of the Required $\beta_{RH}$ at Different $I_L$ Conditions to Meet Routh–Hurwitz Criterion

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Low $I_L$</th>
<th>Moderate $I_L$</th>
<th>High $I_L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_P$, $R_2$</td>
<td>Large</td>
<td>Moderate</td>
<td>Small</td>
</tr>
<tr>
<td>$g_{m2s}$, $g_{m3}$, $g_{mp}$</td>
<td>Small</td>
<td>Moderate</td>
<td>Large</td>
</tr>
<tr>
<td>$\beta_{RH}$ design eqn.</td>
<td>(5.14) and (5.16)</td>
<td>(5.19)</td>
<td>(5.19)</td>
</tr>
<tr>
<td>$\beta_{RH}$ value</td>
<td>Small</td>
<td>Large</td>
<td>Small</td>
</tr>
</tbody>
</table>

Consider the WCF technique employed in the LDO regulator as discussed in Section 5.2, the feedback factor $\beta$ ($\beta_{sim}$) and $R_2f$ are simulated with respect to $I_L$. As can be observed in Fig. 5.6, the WCF technique can significantly reduce $R_2$, especially for moderate and high $I_L$. Moreover, when $I_L$ increases, $\beta_{sim}$ increases to around 25 dB at $I_L = 200 \mu A$ first. Then it drops below 5 dB when $I_L$ is larger than 10 mA.

![Fig. 5.6: Simulated $\beta$ ($\beta_{sim}$) and $R_2f$ at different $I_L$ conditions.](image-url)
To verify that the WCF design can fulfill the stability criterion using numerical examples, the theoretical $\beta_{RH}$ at different $I_L$ conditions are calculated using the right hand side term of inequalities (5.14), (5.16) and (5.19). The design parameters and stability verification using theoretical $\beta_{RH}$ and simulated $\beta_{sim}$ at $I_L = 0$ mA, 1 mA and 50 mA are shown in Table 5.5. It can be seen that the WCF can meet the $\beta_{RH}$ requirement for all three $I_L$ conditions for both $C_L = 470$ pF and 10 nF.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$I_L = 0$ mA</th>
<th>$I_L = 1$ mA</th>
<th>$I_L = 50$ mA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{m1}$ (μS)</td>
<td>51</td>
<td>51</td>
<td>51</td>
</tr>
<tr>
<td>$g_{m2}$ (μS)</td>
<td>24</td>
<td>357</td>
<td>755</td>
</tr>
<tr>
<td>$g_{m3}$ (μS)</td>
<td>71</td>
<td>452</td>
<td>5290</td>
</tr>
<tr>
<td>$g_{mp}$ (μS)</td>
<td>31</td>
<td>2.03e4</td>
<td>3.1e5</td>
</tr>
<tr>
<td>$g_{mc}$ (μS)</td>
<td>131</td>
<td>131</td>
<td>131</td>
</tr>
<tr>
<td>$R_1$ (kΩ)</td>
<td>617</td>
<td>617</td>
<td>617</td>
</tr>
<tr>
<td>$R_2$ (kΩ)</td>
<td>342</td>
<td>22.2</td>
<td>6.46</td>
</tr>
<tr>
<td>$R_p$ (kΩ)</td>
<td>22.4</td>
<td>4.56</td>
<td>0.207</td>
</tr>
<tr>
<td>$C_c$ (pF)</td>
<td>3.5</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>$C_m$ (pF)</td>
<td>0.3</td>
<td>0.3</td>
<td>0.3</td>
</tr>
<tr>
<td>$C_2$ (fF)</td>
<td>26</td>
<td>31</td>
<td>30</td>
</tr>
<tr>
<td>$C_p$ (pF)</td>
<td>2.58</td>
<td>3.22</td>
<td>3.09</td>
</tr>
</tbody>
</table>

Theoretical $\beta_{RH}$ and Simulated $\beta_{sim}$

<table>
<thead>
<tr>
<th>$C_L$</th>
<th>470 pF</th>
<th>10 nF</th>
<th>470 pF</th>
<th>10 nF</th>
<th>470 pF</th>
<th>10 nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\beta_{RH}$ design eqn.</td>
<td>(5.16)</td>
<td>(5.14)</td>
<td>(5.19)</td>
<td>(5.19)</td>
<td>(5.19)</td>
<td>(5.19)</td>
</tr>
<tr>
<td>$\beta_{RH}$ (dB)</td>
<td>−7.5</td>
<td>−29.4</td>
<td>19.5</td>
<td>19.1</td>
<td>0.6</td>
<td>−7.5</td>
</tr>
<tr>
<td>$\beta_{sim}$ (dB)</td>
<td>6</td>
<td>22</td>
<td>3.3</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

From the above analysis together with the numerical examples, the WCF technique can provide an appropriate feedback to meet the Routh–Hurwitz stability criterion for low, moderate and high $I_L$ conditions using the design equations (5.14), (5.16) and (5.19). As a result, these equations provide the design guidelines for the amount of feedback in the WCF at different $I_L$ conditions.
5.4.2. Pole and Zero Locations

The feedback factor $\beta$, $R_{2f}$, poles, zero and related parameters for Large, Moderate and Small $C_L R_O$ cases are presented in Table 5.6. Owing to the cascode compensation, a LHP zero, expressed in (5.10), is generated. It locates outside the unity gain frequency $\omega_{UGF}$. Hence, it will not jeopardize the settling time of LDO regulator. The pole location analysis for each case is discussed as follows:

**Case I – Large $C_L R_O$ (Low $I_L$):** At this condition, $C_L R_O$ forms the low frequency dominant pole ($p_{-3dB} = 1/(C_L R_O)$). Since $p_{-3dB}$ locates at a very low frequency, the $\omega_{UGF}$ is small. At this juncture, all the parasitic poles locate at relative high frequencies. The LDO regulator can maintain a stable operation. This is the reason why a weak negative current feedback can be designed. It also correlates well with the Routh–Hurwitz stability criterion analysis in Section 5.4.1 that at large $C_L R_O$ condition, $\beta_{RH}$ is small using (5.14). In view of the weak feedback, the regulator’s gain and speed do not significantly change with respect to the regulator without WCF technique.

**Case II – Moderate $C_L R_O$ (Low $I_L$):** In this case, $p_{-3dB}$ is constituted by both the $C_L R_O$ and the cascode compensation. The $\omega_{UGF}$ is increased with respect to that in Case I. However, $\omega_{UGF}$ remains small and only half of its maximum value. Besides, $|p_{2,3}|/|p_{-3dB}|$ is also increased slightly when compared to that in Case I. The regulator can achieve a stable operation with a small feedback as suggested in (5.16).

**Case III – Small $C_L R_O$ (Moderate and High $I_L$):** In this case, $p_{-3dB}$ is mainly constituted by the cascode compensation. Moreover, though the loop gain of regulator is reduced by a factor of $\beta$ according to (5.9), the dominant pole $p_{-3dB}$ frequency is increased by the same factor, which yields a constant $\omega_{UGF}$.
### Table 5.6 Feedback Factor $\beta$, Poles, Zero, Q-Factor, $\omega_{UGF}$ for Large, Moderate and Small $C_{1}R_{0}$ Cases

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Case I: Large $C_{1}R_{0}$</th>
<th>Case II: Moderate $C_{1}R_{0}$</th>
<th>Case III: Small $C_{1}R_{0}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Feedback</td>
<td>Low $I_{L}$</td>
<td>Moderate $I_{L}$</td>
<td>High $I_{L}$</td>
</tr>
<tr>
<td>$\beta$</td>
<td>$g_{m1}g_{mf}R_{2}R_{p}+1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_{DC}$</td>
<td>$g_{m1}g_{m2}g_{mp}R_{1}R_{2}R_{p}R_{0}/\beta$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$z_{1}$</td>
<td>$-g_{mc}/C_{c}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{3dB}$</td>
<td>$-1/(C_{1}R_{0})$</td>
<td>$-1/(2C_{1}R_{0})$</td>
<td>$-\beta/(C_{e}g_{m2}g_{mp}R_{2}R_{p}R_{0})$</td>
</tr>
<tr>
<td>$</td>
<td>p_{2,3}</td>
<td>_f$</td>
<td>$\sqrt{\beta g_{mc}/[(\beta C_{c}+C_{p}g_{mc}R_{p})C_{m}R_{1}]}$</td>
</tr>
<tr>
<td>$</td>
<td>p_{4,5}</td>
<td>_f$</td>
<td>$\sqrt{(\beta C_{c}+C_{p}g_{mc}R_{p})/(C_{c}C_{2}C_{p}R_{2}R_{p})}$</td>
</tr>
<tr>
<td>$Q_{p_{2,3}}$</td>
<td>$\sqrt{2(\beta C_{c}+C_{p}g_{mc}R_{p})/(\beta C_{m}g_{mc}R_{1})}$</td>
<td>$\sqrt{\beta C_{m}g_{mc}/(C_{m}g_{m2}g_{mp}g_{mc}R_{2}R_{p})}$</td>
<td></td>
</tr>
<tr>
<td>$Q_{p_{4,5}}$</td>
<td>$\sqrt{\beta C_{2}R_{2}/(C_{p}R_{p})}$</td>
<td></td>
<td>$\sqrt{\beta C_{2}R_{2}/(C_{p}R_{p})}$</td>
</tr>
<tr>
<td>$\alpha_{UGF}$</td>
<td>$g_{m1}g_{m2}g_{mp}R_{1}R_{2}R_{p}/(\beta C_{L})$</td>
<td>$g_{m1}/(2C_{c})$</td>
<td>$g_{m1}/C_{c}$</td>
</tr>
</tbody>
</table>
For \(|p_{2,3}|_f\), they are reduced by a factor of \(\sqrt{\beta}\). However, \(|p_{2,3}|_f\) can still be designed to be higher than that of \(\omega_{UGF}\) through choosing a proper value of \(g_{mc}\) and \(C_c\). This can be derived as

\[
\frac{g_{m2}g_{m3}g_{mp}g_{mc}R_2R_p}{\beta C_mC_L} \geq \frac{g_{m1}}{C_c}
\]

which can be rewritten in a form of

\[
C_c \sqrt{g_{mc}} \geq g_{m1} \sqrt{\frac{\beta C_mC_L}{g_{m2}g_{m3}g_{mp}R_2R_p}}
\]

From (5.21), both \(C_c\) and \(g_{mc}\) can be increased to ensure that \(|p_{2,3}|_f\) locates at a higher frequency than \(\omega_{UGF}\). By substituting the design parameters from Table 5.5 with \(I_L = 1\) mA to (5.21) as a numerical example, the calculated minimum \(C_c\) is 1.5 pF. Since the designed \(C_c\) is 3.5 pF in the WCF LDO regulator, it is more than the required theoretical minimum value.

Of another important design consideration, besides the WCF LDO regulator can fulfill the Routh–Hurwitz stability criterion as discussed in Case III of Section 5.4.1, the open-loop transfer function (5.3) generates a high frequency LHP complex pole pair \(|p_{4,5}|_f\). Its frequency is multiplied by a factor of \(\sqrt{\beta}\) with respect to that without the feedback. In this way, at moderate \(I_L\), due to a large \(\beta\), the complex pole pair \(|p_{4,5}|_f\) is located far away from the \(\omega_{UGF}\). At high \(I_L\), though \(\beta\) is reduced with reference to that at moderate \(I_L\), due to very small \(R_F\) and \(R_2\), the complex pole pair \(|p_{4,5}|_f\) still locates at a much higher frequency than \(\omega_{UGF}\). This confirms the stability of LDO regulator at both moderate and high \(I_L\) conditions.

Figure 5.7 depicts the simulated open-loop gain and phase of the WCF LDO regulator for \(C_L = 470\) pF and \(C_L = 10\) nF under different \(I_L\) conditions. It can be seen
that the LDO regulator can provide a stable operation for both \( C_L \) corners. In addition, the loop gain of the LDO regulator maintains to be more than or equal to 50 dB for different \( I_L \) due to the weighted current feedback mechanism. Thus good regulation accuracy can be achieved.

Fig. 5.7: Simulated open-loop gain and phase at different \( I_L \) for (a) \( C_L = 470 \) pF and (b) \( C_L = 10 \) nF with \( V_{DD} = 0.75 \) V.
Figure 5.8 shows the phase margin (PM) and gain margin (GM) for $C_L = 470 \, \text{pF}$, 1 nF, 3.3 nF and 10 nF when sweeping $I_L$. The regulator achieves a minimum PM of 45° and a minimum GM of 11 dB. This has illustrated that the WCF LDO regulator is stable under different $C_L$ and $I_L$ combinations.

![Phase Margin (PM) and Gain Margin (GM) for different values of $C_L$ and $I_L$.](image)

**Fig. 5.8:** Simulated phase margin (PM) and gain margin (GM) for $C_L = 470 \, \text{pF}$, 1 nF, 3.3 nF and 10 nF when sweeping $I_L$ at $V_{DD} = 0.75 \, \text{V}$.

### 5.4.3. Phase Margin (PM) under $C_L$ and $I_L$ Variations

Refer to the PM plot in Fig. 5.8, for $C_L = 3.3 \, \text{nF}$ and 10 nF, when the $I_L$ increases from 1 μA to 50 mA, the PM of LDO regulator initially decreases to around 45° and then it increases until to 100°. This fact stems from different dominant factors between $C_L R_O$ and cascode compensation term in the formation of $p_{2,3}$. The analysis can also be partitioned into three regions: (i) Under large $C_L R_O$ condition (low $I_L$), due to a small $\omega_{UGF}$, $|p_{2,3}|$ is located at a much higher frequency than $\omega_{UGF}$, resulting in a large PM. (ii) when $I_L$ increases, $R_O$ reduces. The continual reduction of $C_L R_O$ increases the $\omega_{UGF}$. Since the load current $I_L$ is still low, the $|p_{2,3}|$ is almost constant based on Table.
5.6. As such, the PM of regulator will keep reducing as the $\omega_{UGF}$ becomes closer to the $|p_{2,3}|$. When $C_L R_O$ becomes moderate and comparable with cascode compensation term, the PM is approaching to the vicinity of the minimum point. (iii) When $I_L$ further increases, $C_L R_O$ becomes small. On the contrary, the cascode compensation becomes the dominant term, leading to the fixed $\omega_{UGF} (= g_{m1}/C_L)$. Besides, $|p_{2,3}|$ will increase since $g_{mp}$ becomes larger. This will cause the PM to rise when $I_L$ increases.

Based on the analysis in Section 5.4.1, if the feedback factor $\beta$ can meet the design conditions stated in (5.14), (5.16) and (5.19) according to the Routh–Hurwitz stability criterion, $|p_{4,5}|$ will be pushed to a much higher frequency than $\omega_{UGF}$. This indicates that $|p_{4,5}|$ will not influence the PM of regulator. With this assumption, the PM of feedback system can be approximated as

$$ PM \approx 90^\circ - \tan^{-1} \left\{ \frac{\omega_{UGF}}{\frac{Q_{[p_{2,3}]} |p_{2,3}| f}{1 - \left( \frac{\omega_{UGF}}{|p_{2,3}| f} \right)^2}} \right\} + \tan^{-1} \left( \frac{\omega_{UGF}}{z_1} \right) $$

(5.22)

based on [25]. Through substituting the respective expression of $\omega_{UGF}$, $|p_{2,3}|$ and $Q_{[p_{2,3}]}$ for Large, Moderate and Small $C_L R_O$ case in Table 5.6 into (5.22), the design requirement of $\beta_{PM}$ for a minimum PM of $45^\circ$ is analyzed as follows:

**Case (I) – Large $C_L R_O$ (Low $I_L$):** To achieve a PM $\geq 45^\circ$, the necessary condition for $\beta_{PM}$ to be satisfied is

$$ \beta_{PM} \geq \frac{C_m g_{m1} g_{m2} g_{mp} R_L^2 R_1 R_2 R_P}{C_L} $$

(5.23)

From (5.23), the minimum $\beta_{PM}$ ($\beta_{PM_{\text{min}}}$) is inversely proportional to $C_L$. A large $C_L$ gives a smaller $\omega_{UGF}$ which subsequently reduces the feedback requirement for a PM $\geq 45^\circ$.  

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**Case (II) – Moderate $C_L R_O$ (Low $I_L$):** In the situation when the cascode compensation effect equals to that of $C_L R_O$ as defined in (5.15), for a larger $C_L$, a larger $g_{mp}$ (implying a large $I_L$) in the left hand side is needed to balance the right hand side term. This implies that the minimum PM region will shift slightly to the right when $C_L$ increases in context of whole current range (0–50mA). This is consistent with the observation of PM plot in Fig. 5.8. For a PM $\geq 45^\circ$, it suggests that $\beta_{PM}$ should fulfill the condition of 

$$\beta_{PM} \geq \frac{C_m C_p g_{m1}^2 R_1 R_P}{8 C_c^2 (2 + g_{m1}/g_{mc}) C_d C_m g_{m1} R_I}$$

(5.24)

It is noted that $I_L$ is still small even the balance point for (5.15) shifts to a higher $I_L$ when $C_L$ increases. Moreover, since $R_P$ is inversely proportional to $\sqrt{I_L S_{d1}/S_p}$, where $S_p$ and $S_{d1}$ is the respective aspect ratio of the power transistor $M_P$ and the driving transistor $M_{d1}$ in Fig. 5.3, $R_P$ is approximated independent of $C_L$. As a result, $\beta_{PM, min}$ is almost constant for the whole $C_L$ range from (5.24).

**Case (III) – Small $C_L R_O$ (Moderate and High $I_L$):** As indicated in small $C_L R_O$ case of Table 5.6, $|p_{2,3}|$ is inversely proportional to $\sqrt{\beta}$. $\beta$ should not be made too large to achieve a minimum $45^\circ$ PM. The condition for the $\beta_{PM}$ becomes 

$$\beta_{PM} \leq \frac{C_c g_{mc} g_{m2}^2 g_{m3} g_{mp}^2 R_2^2 R_P}{C_m C_L g_{m1}^2}$$

(5.25)

From (5.25), the maximum allowable $\beta_{PM}$ ($\beta_{PM, max}$) is proportional to $g_{mp}$. At small $C_L R_O$ case, due to large $I_L$, $g_{mp}$ becomes large, contributing a large $\beta_{PM, max}$. On the other hand, due to the WCF technique to reduce the feedback at large $I_L$, the design $\beta$ is not easily exceeding the $\beta_{PM, max}$ defined in (5.25).
To verify the WCF regulator can fulfill the design requirement for a minimum 45° PM using numerical examples, $\beta_{PM\_min}$ or $\beta_{PM\_max}$ at different $C_L R_O$ conditions are calculated using (5.23)–(5.25). Using the design parameters in Table 5.5, the theoretical $\beta_{PM}$ and simulated $\beta_{sim}$ for Large, Moderate and Small $C_L R_O$ are shown in Table 5.7. It is noted that (i) for Large $C_L R_O$ case, $\beta_{PM}$ at $C_L = 3.3$ nF and $I_L = 0$ mA is chosen. This is because, for $C_L = 470$ pF and 1 nF, the $C_L R_O$ is already comparable with the cascode compensation term at 0 mA. For 10 nF, $\beta_{PM\_min}$ is smaller than that of 3.3 nF. (ii) For Moderate $C_L R_O$ case, the worst $\beta_{PM}$ at $C_L = 470$ pF, $I_L = 0$ mA is chosen. (iii) For Small $C_L R_O$ cases, the $\beta_{PM}$ at $C_L = 10$ nF, $I_L = 50$ mA is chosen. The results in Table 5.7 indicate that the WCF can meet the $\beta$ requirement for all three $C_L R_O$ conditions. A minimum PM of 45° can be achieved as depicted in Fig. 5.8.

**Table 5.7 Numerical Example for PM Verification Using Theoretical $\beta_{PM}$ and Simulated $\beta_{sim}$**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Large $C_L R_O$</th>
<th>Moderate $C_L R_O$</th>
<th>Small $C_L R_O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_L$</td>
<td>3.3 nF</td>
<td>470 pF</td>
<td>10 nF</td>
</tr>
<tr>
<td>$I_L$</td>
<td>0 mA</td>
<td>0 mA</td>
<td>50 mA</td>
</tr>
<tr>
<td>$\beta_{PM_Design_Eqn.}$</td>
<td>(23)</td>
<td>(24)</td>
<td>(25)</td>
</tr>
<tr>
<td>$\beta_{PM_dB}$</td>
<td>-2.9</td>
<td>3.3</td>
<td>50.6</td>
</tr>
<tr>
<td>$\beta_{sim_dB}$</td>
<td>6</td>
<td>6</td>
<td>3.3</td>
</tr>
<tr>
<td><strong>Criterion For 45° PM</strong></td>
<td>$\beta_{sim} \geq \beta_{PM}$</td>
<td>$\beta_{sim} \geq \beta_{PM}$</td>
<td>$\beta_{sim} \leq \beta_{PM}$</td>
</tr>
<tr>
<td><strong>Meet Criterion</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Simulated PM</strong></td>
<td>63°</td>
<td>52°</td>
<td>97°</td>
</tr>
</tbody>
</table>

In brief, for regulator’s stability, both the Routh–Hurwitz stability criterion and 45° minimum PM should be fulfilled. By combining the design equations of $\beta_{RH}$ in Section 5.4.1 [(5.14), (5.16) and (5.19)] and $\beta_{PM}$ in Section 5.4.3 [(5.23)-(5.25)], the required $\beta$ is summarized in Table 5.8. For large $C_L R_O$ case (Case I), since $C_m R_1 \gg C_c g_{mc}$, if the condition in (5.23) is met, (5.14) is valid as well. This suggests that
(5.23) is the only choice for design inequalities. For Moderate $C_L R_O$ case (Case II), the design equations are decided by (5.16) and (5.24) together. For small $C_L R_O$ case (Case III), (5.19) and (5.25) gives the lower and upper bound for $\beta_{req}$ respectively. Using this table, the design guidelines for $\beta$ is investigated in details.

### Table 5.8 Combined $\beta$ Design Inequalities Using $\beta_{RH}$ and $\beta_{PM}$

<table>
<thead>
<tr>
<th>Case</th>
<th>$\beta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$\beta \geq \frac{C_m g_{m1} S_m g_{m2} R_1^2 R_p R_p}{C_L}$</td>
</tr>
<tr>
<td>II</td>
<td>$\left[\beta &gt; \frac{C_p g_{m1} R_p}{(2C_c)}\right]$ &amp; $\left[\beta \geq \frac{C_m C_p g_{m1}^2 R_p R_p}{8C_c^2 - (2 + \frac{g_{m1}}{g_{mc}}) C_m C_p g_{m1} R_1}\right]$</td>
</tr>
<tr>
<td>III</td>
<td>$\frac{C_2 g_{m2} S_m g_{mp} R_2^2 R_p}{C_L} + \left(1 + \frac{g_{m1}}{g_{mc}}\right) \frac{C_p g_{mc}^2 R_p}{C_m} &lt; \beta \leq \frac{C_2 g_{mc} S_m g_{m2} S_m g_{mp} R_2^2 R_p}{C_m C_L g_{m1}^2}$</td>
</tr>
</tbody>
</table>

Case I: Large $C_L R_O$ using (5.23). Case II: Moderate $C_L R_O$ using (5.16) and (5.24). Case III: Small $C_L R_O$ using (5.19) and (5.25).

### 5.4.4. Combined Frequency Compensation and Q-Factor

The WCF LDO regulator employs a combined cascode and Miller compensation. The dominant pole is determined by the cascode compensation since it can push the non-dominant pole to a higher frequency under a large capacitive load in comparison to the Miller compensation counterpart [100]. Unfortunately, the cascode compensation easily gives gain peaking due to a large parasitic Q factor [101]. To overcome the drawback, a small Miller compensation capacitor is added in this LDO regulator so as to reduce the Q factor. This is mainly because the Q factor value is inversely proportional to the capacitance at the Miller node [101]. This can also be validated from the Q factor expressions shown in Table 5.6. At moderate and high $I_L$ conditions (cascode compensation dominating), $Q_{[\beta,R]}$ is inversely proportional to $\sqrt{C_c}$. 
A large $C_m$ contributes to a small $Q$ factor which can reduce the peaking effect arising from the complex pole pair $|p_{2,3}|$. However, a large $C_m$ will reduce the frequency of $|p_{2,3}|$ as well. This will jeopardize the cascode effect. For this reason, $C_m$ is designed to be small (0.3 pF) in the WCF topology to achieve a reasonable $Q$ factor whilst keeping the complex pole pair $|p_{2,3}|$ locating outside the $\omega_{UGF}$.

5.4.5. Minimum $C_L$ for a Stable Operation

As discussed in Section 5.4.3, when $C_L$ is 470 pF, the dominant pole is in moderate $C_L R_O$ region at $I_L = 0$ mA. If the minimum $C_L$ (470 pF) is further reduced to a smaller value, the dominant pole will directly move into small $C_L R_O$ region. To meet the Routh–Hurwitz stability criterion, $\beta_{RH}$ must fulfill (5.19) across the whole $I_L$ range. However, at small $I_L$, $R_P$ becomes large and it causes a large $\beta_{RH}$. This suggests that a very strong feedback is needed at low $I_L$ to ensure stable operation. The gain as well as the speed of regulator will be limited. Based on the tradeoff design considerations, the output $C_L$ of regulator is preferably to start from the mid-range capacitive load (470 pF) onwards.
5.5. Circuit Implementation and Power Supply Rejection Analysis

5.5.1. Schematic Implementation

The complete schematic implementation of the WCF LDO regulator is shown in Fig. 5.9. The red arrows indicate the power supply noise injection paths. It utilizes a folded cascode error amplifier constituted by (M₀ – M₈) as the first gain stage. The 2\textsuperscript{nd}, 3\textsuperscript{rd} inverting gain stages and the WCF block employ the same structure as that in Fig. 5.3. The overshoot reduction block (C₉, R₉, M₁₃) senses the voltage swing at the node Nₚ and generates a momentary sinking current to reduce the overshoot magnitude as well as settling time of the LDO regulator.

To compare the regulation accuracy and the speed of LDO regulator with the two proposed NCF and WCF technique, a NCF LDO regulator is also built and simulated. In the NCF LDO regulator, Mₐ₃ in the WCF block (Fig. 5.9) is removed. In such an arrangement, both Mₐ₁ and Mₐ₂ are working in saturation region. This turns out that the negative current feedback is kept strong for both moderate and high Iₗ conditions. Figure 5.10 shows the exemplary transient responses of the LDO regulator with NCF and WCF technique. Under the same load current switching condition, it can be observed that the WCF LDO regulator displays a 1.5 times smaller undershoot and overshoot, and an approximate 2 times better load regulation with respect to the NCF LDO regulator. This has demonstrated that the WCF technique addresses the limitations of the NCF and achieves a better optimization of stability, accuracy and speed.
Fig. 5.9: Schematic of the WCF LDO regulator.
As shown in Fig. 5.9, assumed that the supply noise is $\Delta V_{DD}$, the analysis for each path is discussed as follows:

For path 1 and path 2, as discussed in [95], the supply ripple is reflected at node $N_1$. It can be expressed as

\[
\Delta V_{N_1} = \frac{\Delta V_{DD}}{R_{ds8}} (R_{ds8} / g_{m6} R_{ds6} R_{ds4}) + \frac{\Delta V_{DD}}{R_{ds8} (1 + g_{m6} R_{ds6} R_{ds4})} 
\]

\[
\approx \frac{\Delta V_{DD}}{R_{ds8}} 
\]

\[
= \Delta V_{DD} 
\]

(5.26)

For path 3, since the gate voltage variation of $M_9$ equals to its source voltage variation, the supply noise coming from paths 1-3 cancel each other. Thus, $\Delta V_{N2}$ due to path 1-3 equals to zero. Another noise path contributes to node $N_2$ is coming from the WCF circuit (path 6 and 7). As discussed in Section 5.2 and 5.3, at small $I_L$, $g_{mf}$ is small. The noise contribution for WCF is small as well. At moderate $I_L$, $g_{mf}$ increases,
the noise contribution at node $N_2$ can be expressed as $\Delta V_{N_2_{wcf}} = -g_{out} \Delta V_{DD} R_{2f}$. Since the feedback reduces the impedance $R_{2f}$, $\Delta V_{N_2_{wcf}}$ is small as well. Finally, at high $I_L$, both $g_{out}$ and $R_{2f}$ are small. $\Delta V_{N_2_{wcf}}$ is also small. Therefore, the supply noise at node $N_2$ can be approximated as zero due to path 1-3 and path 6-7.

Refer to path 4 and path 5, since $R_X + 1/g_{m12} \ll R_{ds11}$, the noise at node $N_P$ can be expressed as

$$\Delta V_{NP} = \frac{R_{ds11}}{R_{ds11} + R_X + 1/g_{m12}} \Delta V_{DD}$$

$$\approx \Delta V_{DD}$$

(5.27)

Finally, for path 8, there are two ways for the supply noise coming into the output. The first way is to vary the $V_{SG}$ of the power transistor $M_P$. As shown in (5.27), the gate voltage variation of $M_P$ equals to the source voltage variation. The supply noise contribution due to $\Delta V_{SG}$ of $M_P$ can be approximated as zero. The second way is due to the limited $R_{dsp}$ for $M_P$. The limited $R_{dsp}$ forms a resistor-divider with the regulated output impedance and injects parts of the supply noise into $V_{OUT}$. As a result, based on the analysis method in [95], the PSR of the WCF LDO regulator can be expressed as

$$PSR = \frac{\Delta V_{OUT}}{\Delta V_{DD}}$$

$$= \frac{\left( z_{out} \parallel z_{out\_reg} \right)}{\left( z_{out} \parallel z_{out\_reg} \right) + R_{dsp}}$$

(5.28)

where

$$z_{out} = R_L \parallel \left( \frac{1}{sC_L} \right)$$

$$z_{reg} = \frac{z_{out} \parallel R_{dsp}}{A(s)}$$

$$A(s) = \frac{A_{dc}}{1 + s/p_{-3dB}}$$

(5.29)
It is noted that the loop gain transfer function in (5.3) is simplified as a one-pole system within the unity gain frequency (UGF).

At low frequency, \( A(s) \gg 1 \), and \( R_L \gg 1/sC_L \), from (5.28) and (5.29), the PSR of the regulator can be expressed as

\[
PSR \approx \frac{z_{\text{out, reg}}}{z_{\text{out, reg}} + R_{\text{dsp}}} \\
\approx \frac{R_L (1 + s/p_{-3\text{dB}}) / A_{DC}}{R_L (1 + s/p_{-3\text{dB}}) / A_{DC} + R_{\text{dsp}}} \\
\approx \frac{R_L (1 + s/p_{-3\text{dB}})}{A_{DC} R_{\text{dsp}}} \quad (5.30)
\]

As indicated in (5.30), the regulator shows a PSR inversely proportional to the DC gain of the feedback loop. It also depicts a zero at \( p_{-3\text{dB}} \). This is because the loop gain starts to decrease after \( p_{-3\text{dB}} \) which reduces the output impedance reduction effect.

At moderate frequency when \( A(s) \) is smaller or equal to 1, the feedback loop no longer reduces the impedance. In this frequency range, \( R_L \gg 1/sC_L \), it yields a PSR of

\[
PSR \approx \frac{z_{\text{out}}}{z_{\text{out}} + R_{\text{dsp}}} \\
\approx \frac{R_L}{R_L + R_{\text{dsp}}} \quad (5.31)
\]

At high frequency when \( R_L \) is smaller than \( 1/sC_L \), \( z_{\text{out}} \) is dominated by \( C_L \), the PSR of the LDO regulator can be derived as

\[
PSR \approx \frac{z_{\text{out}}}{z_{\text{out}} + R_{\text{dsp}}} \\
\approx \frac{1/(sC_L)}{1/(sC_L) + R_{\text{dsp}}} \\
= \frac{1}{1 + sC_L R_{\text{dsp}}} \quad (5.32)
\]

As indicated in (5.32), the PSR will become smaller when the frequency is further increased. This is because, when the frequency increases, the output capacitor
functions as a very small impedance reference to ground. Thus, the noise at the output becomes smaller when the frequency increases.

Figure 5.11 depicts the simulated PSR for $I_L = 0, 1$ mA, $10$ mA, $25$ mA and $50$ mA for $C_L = 470$ pF. It can be seen that PSR responses follows the theoretical predication trends and validates the PSR analysis. (i) At low frequency, the PSR of the LDO regulator is determined by the feedback loop gain and displays a zero around $f_{3dB}$. The low frequency PSR at 1 mA is worse than that at other $I_L$ due to the strong loop gain reduction by the WCF. (ii) At moderate frequency, without the feedback loop to reduce the impedance, the PSR of the regulator approaches to the worst point. (iii) At high frequency, the PSR becomes smaller due to the output capacitor filtering effect. For a larger $I_L$, $R_{ dsp}$ becomes smaller, thus the PSR will becomes better at a higher frequency as indicated in (5.32) and Fig. 5.11.

Fig. 5.11 Simulated PSR for $C_L = 470$ pF under different $I_L$. 
5.6. Experimental Results and Discussions

The WCF LDO regulator is implemented using UMC 65-nm CMOS process. The microphotograph of the WCF regulator is shown in Fig. 5.12. Excluding the supply and output PADs as connectors, the active area is 0.0133 mm$^2$. To reduce the offset, common centroid layout matching technique is employed in the differential pair input transistors ($M_1$ and $M_2$) and all the current mirrors of Fig. 5.9. As for the power transistor, multi-finger layout in Section 3.5.2 (Fig. 3.10) and the metallization technique in Section 3.5.3 (Fig. 3.13) are utilized to minimize the parasitic effect.

At a 0.75 V supply voltage, the WCF LDO regulator can support a maximum $I_L$ of 50 mA. The dropout voltage is less than 0.2 V at full $I_L$. The measured quiescent current at zero $I_L$ is 15.9 $\mu$A. With a total 3.8 pF (3.5 pF cascode + 0.3 pF Miller) compensation capacitance, the WCF LDO regulator offers stable operation for $C_L$ ranging from 470 pF to 10 nF across the whole $I_L$ range.

![Fig. 5.12: Microphotograph of the WCF LDO regulator.](image)

It is noted that external reference voltages are used and off-chip capacitors are added to model the $C_L$ of the LDO regulator during the measurement. To test the
stability and the performance of the WCF LDO regulator for the whole $C_L$ range, four standard load capacitors (470 pF, 1 nF, 3.3 nF and 10 nF) have been chosen. In addition, two $I_L$ switching cases (0 to maximum $I_L$ and 1 mA to maximum $I_L$) are used to measure the transient performance.

Figure 5.13 shows the measured load transient responses of the WCF LDO regulator when $I_L$ is switching from 0 to 50 mA with an edge time of 100 ns for all four load capacitors. The supply voltage is 0.75 V and the output voltage is 0.55 V. As can be observed from the graphs, the undershoots are 113 mV, 109 mV, 98 mV, 72 mV whereas the overshoots are 29 mV, 29 mV, 27 mV, 32 mV for $C_L = 470$ pF, 1 nF, 3.3 nF and 10 nF, respectively. The undershoot becomes smaller when the load capacitor increases. This is because a larger capacitor is able to absorb a larger transient current during $I_L$ switching. In addition, due to the intelligent control of WCF and the high speed property of the 3$^{rd}$ gain stage, the settling time of the WCF LDO regulator is quite small. The measured settling time are 248 ns, 244 ns, 252 ns and 368 ns for $C_L = 470$ pF, 1 nF, 3.3 nF and 10 nF, respectively.
Fig. 5.13: Measured load transient responses with $V_{\text{DD}} = 0.75\,\text{V}$, $V_{\text{OUT}} = 0.55\,\text{V}$ for (a) $C_L = 470\,\text{pF}$, (b) $C_L = 1\,\text{nF}$, (c) $C_L = 3.3\,\text{nF}$ and (d) $C_L = 10\,\text{nF}$. 
Figure 5.14 shows the transient responses of the WCF LDO regulator at $V_{DD} = 0.75$ V when $I_L$ switches from 1 mA to 50 mA (vice versa) for $C_L = 470$ pF and $C_L = 10$ nF. Using an identical edge time of 100 ns, the undershoots are substantially reduced when compared with that of $I_L$ switching from 0 to 50 mA. The undershoots are 24 mV, 35 mV whereas the overshoots are 24 mV, 29 mV for $C_L = 470$ pF and 10 nF, respectively.

![Figure 5.14: Measured load transient responses at $V_{DD} = 0.75$ V with $I_L$ switching from 1 mA to 50 mA (vice versa) for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF.](image)

Figure 5.15 depicts the transient responses of the WCF LDO regulator at $V_{DD} = 1.2$ V when $I_L$ switches from 1 mA to 50 mA (vice versa) for $C_L = 470$ pF and $C_L = 10$ nF. The LDO regulator works well for a 1.2 V supply. Comparing the results with $V_{DD} =$
0.75 V in Fig. 5.14, the undershoot and overshoot increase by around 15 mV. This is because, at $V_{DD} = 1.2$ V, the large feedback transistor $M_a2$ turns off at a higher $I_L$ than that of $V_{DD} = 0.75$ V. Therefore, the regulator’s speed at high $I_L$ is slightly reduced. This leads to a small amount increment for transient undershoot and overshoot.

![Diagram showing load transient responses](image)

**Fig. 5.15**: Measured load transient responses at $V_{DD} = 1.2$ V with $I_L$ switching from 1 mA to 50 mA (vice versa) for (a) $C_L = 470$ pF and (b) $C_L = 10$ nF.

The line transient response at $I_L = 1$ mA, $C_L = 470$ pF is depicted in Fig. 5.16. When $V_{DD}$ switches from 0.75 V to 1.2 V with a 10 µs edge time, the maximum output voltage spike is 4.3 mV and the introduced increment of error voltage is only 1.8 mV.

To measure the power supply rejection of the LDO regulator, a measurement setup shown in Fig. 5.17 is used. A spectrum analyzer is utilized to generate an AC sine wave signal with different frequencies and to capture the output voltage variation. The
PSR of LDO regulator can be calculated by dividing the output and input voltages. The magnitude of the input sine wave is set to be 31 mV which will not force the LDO regulator moving into dropout region. Figure 5.18 shows the measured power supply rejection (PSR) of the WCF LDO regulator for \( C_L = 470 \) pF at different \( I_L \) conditions. At 1 kHz, it can be seen that the minimum PSR is around -44 dB when \( I_L = 1 \) mA. This is due to some loop gain reduction from the large feedback (\( \beta \)) as revealed in (5.9). At full \( I_L \), the regulator achieves a PSR of -51 dB. Figure 5.19 depicts the measured output noise response of the LDO regulator at \( C_L = 470 \) pF and \( I_L = 0 \) mA. It can be seen that the noise is -98.7 dBm/Hz (2.6 \( \mu \)V/\( \sqrt{\text{Hz}} \)) at 100 Hz and -105 dBm/Hz (1.25 \( \mu \)V/\( \sqrt{\text{Hz}} \)) at 100 kHz, respectively.

![Fig. 5.16: Measured line transient response at \( I_L = 1 \) mA and \( C_L = 470 \) pF.](image-url)
Fig. 5.17: PSR measurement setup.

Fig. 5.18: Measured PSR at $C_L = 470$ pF for different $I_L$. 
Performance comparison between the WCF LDO regulator and the other reported state-of-the-art OCL-LDO regulators is presented in Table 5.9. With the WCF circuit technique, the LDO regulator achieves good performance metrics with an additional merit to drive a wide $C_L$ range. To compare the load transient performance, the OCL-LDO regulator figure-of-merit (FOM) expressed in (4.15) of Section 4.4.2 is adopted.

To provide a comparison, all the results in Table 5.9 for the WCF LDO regulator is based on $C_L = 470 \text{ pF}$ which is regarded as the closer load capacitance value with respect to the reported works. Since some of the designs [23, 24] were tested using some amount of minimum loading currents, two FOMs of the WCF LDO regulator are used for comparison. The first FOM (left column) represents the performance metric for $I_L$ switching from 0 to 50 mA while the second FOM (right column) represents the performance metric for $I_L$ switching from 1 mA to 50 mA.

Fig. 5.19: Measured Output Noise at $C_L = 470 \text{ pF}$ with 0 mA $I_L$. 

![Graph of measured output noise at CL = 470 pF with 0 mA IL.](image)
**Table 5.9 Performance Comparison with the Reported OCL-LDO Regulators**

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<tr>
<th>Parameter</th>
<th>[18]</th>
<th>[21]</th>
<th>[23]</th>
<th>[24]</th>
<th>[26]</th>
<th>[27]</th>
<th>[28]</th>
<th>[29]</th>
<th>[30]</th>
<th>[31]</th>
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<td>0.35</td>
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<td>0.11</td>
<td>0.065</td>
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<td>2.5-4</td>
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* Quiescent current includes the current consumption of bias circuit.  † The minimum I<sub>L</sub> used to test the transient performance.  # Estimated area.
As can be seen from Table 5.9, the WCF LDO regulator design achieves a comparable or better FOM with respect to the reported OCL-LDO regulators. In addition, it can drive a wide $C_L$ range with fast settling time and good performance metrics such as load regulation, line regulation and PSR.
5.7. Summary

A Type-II OCL-LDO regulator using weighted current feedback (WCF) technique is proposed in this Chapter. It establishes a weighted negative current feedback loop and provides an adaptive bias to the inter-gain stage. This permits smart management of the output impedance and gain of the inter-gain stage. As a result, using the WCF circuit technique and Routh–Hurwitz stability criterion to devise the design strategy and access the stability, the regulator can achieve stable operation, high accuracy and fast response simultaneously with small quiescent power consumption.

Validated by UMC 65-nm CMOS process, the simulation and measurement results have demonstrated that the WCF technique can stabilize the LDO regulator for load capacitance ranging from 470 pF to 10 nF whilst maintaining a very good transient performance metrics. The WCF regulator design reaches a comparable or better FOM with respect to the reported OCL-LDO regulators. Therefore, the WCF LDO regulator topology is useful for fully on-chip applications with wide load capacitance range.

Figure 5.20 gives an overall comparison of the performance metric using the maximum $C_L$ versus quiescent current for the reported OCL-LDO regulators and the proposed Type-I and Type-II LDO regulators. For Type-I LDO regulator, under a quiescent current of 23.7 $\mu$A and a supply of 1.2 V, it achieves an undershoot of 40 mV and an overshoot of 19 mV when $I_L$ is switching from 0 mA to 50 mA in 100 ns. The settling time is 1.65 $\mu$s. Based on Table 4.7, the Type-I LDO regulator offers one of the smallest undershoot/overshoot and settling time. Thus, the FOM of Type-I LDO regulator are significantly better or comparable with other reported designs whilst it supporting the widest $C_L$ range. Regarding the Type-II LDO regulator, under a quiescent current of 15.9 $\mu$A and a supply of 0.75 V, it displays an undershoot of 113
mV and an overshoot of 29 mV when $I_L$ is switching from 0 to 50 mA in 100 ns. The settling time of this LDO regulator is only 250 ns. Based on Table 5.9, the Type-II LDO regulator achieves one of the smallest settling time. It also offers better or comparable FOM with respect to other LDO topologies. Therefore, it has demonstrated that both regulators have achieved wide $C_L$ range driving ability whilst featuring small quiescent power and fast transient speed. As such, these two LDO regulators contribute the main part of this research work. They are useful for fully on-chip power management applications.

Fig. 5.20: Maximum load capacitance versus quiescent current for the reported OCL-LDO regulators and the proposed two wide $C_L$ range LDO regulators.
In this Chapter, a review of reported PVT compensation techniques for digital circuit systems is firstly introduced. Then, a fully on-chip PVT compensated supply (PVTCS) which is targeted for point-of-load digital system is proposed. The working principle, circuit implementations, simulation and measurement results and performance comparison are presented and discussed in details.

6.1. Review of PVT compensation techniques

As discussed in Chapter 1, as technology scales down, the digital circuit performance exhibits high sensitivity to PVT variations. To tackle this issue, an adaptive body bias and adaptive supply control can be applied. For the adaptive bias technique, the threshold voltage ($V_{TH}$) of the devices can be adjusted accordingly through modifying the body voltage of the transistors. This turns out that the current and the speed or delay of the digital circuits can be changed. The prior-art adaptive body bias techniques are discussed as follows.

A bidirectional adaptive body bias technique is utilized in [51] to reduce the die-to-die (D2D) and within-die (WID) variations, with the circuit architecture shown in Fig. 6.1. As indicated, a target precision clock signal $\phi$ which represents the desired working frequency of the circuit is applied externally. The critical path output is then compared with $\phi$ through a phase detector. The comparison output “PD” is used to clock a 5-bit counter whose output is converted to a body bias voltage $V_{BP}$. Using this $V_{BP}$, the body voltage of the PMOS transistors in the digital load circuit as well as the critical path in Fig. 6.1 is adjusted simultaneously. Finally, the speed of digital load circuit can be set according to the designed clock frequency. This method is simple and effective, the measurement results have shown that it can reduce the die frequency variation by a factor of seven (85.7%).

Fig. 6.1: Block diagram of adaptive body bias for reducing impacts of Die-to-Die and Within-Die parameter variations [51].
6.1.2. Mixed Body Bias Technique with Fixed $V_{TH}$ and $I_{ds}$ Generation Circuits

In this method, a body bias control is applied on both the NMOS and PMOS transistors to ensure the $V_{TH}$ and saturation current ($I_{ds}$) are fixed [46]. The fixed $V_{TH}$ and $I_{ds}$ generator is shown in Fig. 6.2. A bandgap voltage reference (BGR) generates two reference voltages to define $V_{gsn}$ and $V_{gsp}$. Meanwhile, a current generator (CG) generates the adequate current to bias the body bias generator (BBG). Since the body voltage of the NMOS can be a negative value, a negative bias voltage generator (NBG) is realized by using a charge pump circuit. The simplified schematic of the BBG is depicted in Fig. 6.3, the body voltage $V_{bn}$ is adjusted such that the $V_{GS}$ of the NMOS transistor is equal to the constant $V_{gsn}$ at a bias current of CGN1. The same goes for the PMOS transistors. The generated $V_{bn}$ and $V_{bp}$ will be applied to the digital circuits. As a consequence, the transistor’s $V_{TH}$ and $I_{ds}$ are fixed and the digital circuit's speed is constant. This circuit technique is targeted for reducing the temperature variation of the digital circuits. The measurement results have proved that it can reduce the delay.

Fig. 6.2: Fixed $V_{TH}$ and $I_{ds}$ generator [46].
variation by 85% under temperature variation when compared with the normal body bias technique.

6.1.3. On-chip PVT Compensation Technique Using Current Monitoring Circuit

An on-chip PVT compensation technique using a current monitoring circuit is reported in [45] as illustrated in Fig. 6.4. The $V_{TH0}$ generator in [63] is used to generate a constant current $I_{REF}$ [74] which is then is applied to the replica NMOS and PMOS diode transistors. Through a DC-DC converter which works as a buffer, the supply of the digital circuits is set to be equal to $V_{GS}$ of NMOS diode transistor ($V_{GSN} = V_{REF}$). Turing to the PMOS transistor, under the same bias current of $I_{REF}$, the body voltage $V_{BP}$ is adjusted such that the $V_{GS}$ of PMOS diode ($V_{GSP}$) is equal to $V_{GSN}$ and $V_{REF}$. The body voltage $V_{BP}$ is then applied to drive the body of the PMOS transistors in digital circuits. With this implementation, the current of NMOS and PMOS transistors in digital circuits are kept constant (= $I_{REF}$) irrespective to the process and temperature variations. As such, the speed variations of the digital circuit can be reduced. The simulation results have revealed that it can
improve the performance by 71% and 90.4% under the process and temperature variations.

In this compensation system, a switching DC-DC converter is utilized to power up the digital circuits and a substrate bias to compensate the variation of PMOS transistors. The switching regulator may limit the speed of response and increase the complexity, hence leading to the increase of silicon area in this compensation architecture.

Fig. 6.4: Schematic of the on-chip PVT compensation system [45].
6.1.4. PVT Compensation Using Adaptive Supply Control

As technology scales down, the effectiveness of body bias to control the $V_{TH}$ of the devices is reduced due to a smaller body factor. Together with the potential latch up problem and the high leakage effect under high operating temperature, the application of adaptive body bias technique to reduce PVT variations is limited. Another compensation method is to adaptively change the supply of the digital circuit through post-silicon trimming [78, 79]. This method is effective but the cost is increased due to the post-silicon trimming process.

In brief, both the adaptive body bias and the adaptive supply control can compensate the PVT variations of the digital circuits. However, the inherent limitations of body bias including reduced body bias factor, potential latch up problem and high leakage limit its applications for modern CMOS technology. The adaptive supply control is another effective method to perform PVT compensation but an on-chip circuit topology is needed. In view of that, a fully on-chip PVT compensation supply (PVTCS) is proposed and discussed in the subsequent sections.
6.2. Proposed PVT Compensated Supply (PVTCS)

In this section, the operation principle, circuit implementation, simulation and measurement results, performance comparison and discussions are presented for the proposed PVTCS system.

6.2.1. Operation Principle

The circuit architecture of PVTCS with the load circuits is depicted in Fig. 6.5. It contains a reference block that generates both voltage and current references, two separate biased PMOS and NMOS (P/N) diodes to sense the process and temperature variation of the digital circuits, a three-port differential difference amplifier (DDA) to generates an accurate weight and to perform subtraction and addition functions, a LDO regulator to drive the digital load circuit and a digitally-tracked oscillator which models as a digital load. The reference block provides a reference voltage ($V_{\text{REF}/2}$) for the DDA. It also generates two reference currents (both equal to $I_{\text{REF}}$) to bias the respective P and N diode. The DDA compares the reference voltage $V_{\text{REF}/2}$ with respect to half of gate-to-source voltage of $V_{\text{GSN}/2}$ and half of source-to-gate voltage $V_{\text{SGP}/2}$. It aims to generate a PVT compensated $V_R$ for the LDO regulator. Finally, the high speed LDO regulator serves as a buffer and provides the supply to power the digital circuit. This load circuit is modeled by the digital tracked oscillator in form of a chain of inverters or combinations of logic gates so as to evaluate the performance under PVTCS. Similar to [45], the process and temperature compensation principles are analyzed using the delay model of a CMOS inverter chain. It is shown in the following.
6.2.1.1. Process Variation Compensation

From the Alpha-Power law MOSFET Model [47], the delay of a CMOS inverter $t_d$ ($t_{pLH}$, $t_{pHL}$) can be expressed as

$$t_d \approx \left[ \frac{1}{2} - \frac{1 - (V_{TH}/V_{DD})}{1 + \alpha} \right] t_T + \frac{C_d V_{DD}}{2I_D}$$  \hspace{1cm} (6.1)$$

where $t_T$ is the transition time of input waveform, $\alpha$ is the velocity saturation index. $I_D$ is the saturation current of MOSEFT which is given as

$$I_D = \beta (V_{GS} - V_{TH})^\alpha$$  \hspace{1cm} (6.2)$$

where $\beta$ is defined as $0.5 \mu(T) C_{OX} (W/L)$, $\mu(T)$ is the mobility of the electrons or holes in which $T$ is the operating temperature, $C_{OX}$ is the gate oxide capacitance. In comparison, the mobility of electrons and holes and their velocity saturation indexes are much less variation with respect to that of the threshold values. Therefore, $\beta$ in (6.2) can be approximated as a constant under process variation. Besides, for a fast digital system, $t_T$ is small. Since $V_{GS}$ in (6.2) can be approximated as $V_{DD}$, $t_d$ in (6.1) can be simplified as
\[ t_d \approx \frac{C_L V_{DD}}{2\beta (V_{DD} - V_{TH})^a} \]  

(6.3)

In order to maintain the delay of an inverter chain as a constant under the scenario of process variation, \( t_{pLH} + t_{pHL} \) must be kept constant, which are translated into the following relationship:

\[
t_{pHL} + t_{pLH} = \frac{C_L V_{DD1}}{2\beta_N (V_{DD1} - V_{THN1})^{a_N}} + \frac{C_L V_{DD1}}{2\beta_P (V_{DD1} - V_{THP1})^{a_P}}
\]

\[
= \frac{C_L V_{DD2}}{2\beta_N (V_{DD2} - V_{THN2})^{a_N}} + \frac{C_L V_{DD2}}{2\beta_P (V_{DD2} - V_{THP2})^{a_P}}
\]

(6.4)

where \( V_{DD1}, V_{THN1} \) and \( V_{THP1} \) are the supply voltage and the threshold voltages for NMOS and PMOS at typical process corner respectively. \( V_{DD2} \) is the compensated supply voltage. \( V_{THN2} \) and \( V_{THP2} \) are threshold voltages for NMOS and PMOS under process variation. From (6.4), the added compensation supply voltage \( \Delta V_{DD} \) can be obtained as

\[
\Delta V_{DD} = V_{DD2} - V_{DD1}
\]

\[
\approx \frac{\alpha_P \Delta V_{THP} + \gamma \alpha_N \Delta V_{THN}}{\gamma \alpha_N + \alpha_P}
\]

(6.5)

where

\[
\Delta V_{THP} = V_{THP2} - V_{THP1},
\]

\[
\Delta V_{THN} = V_{THN2} - V_{THN1},
\]

\[
\gamma = \frac{\beta_P (V_{DD1} - V_{THP1})^{a_P + 1}}{\beta_N (V_{DD1} - V_{THN1})^{a_N + 1}}.
\]

\[
D = \frac{\gamma \alpha_N}{\gamma \alpha_N + \alpha_P}
\]

(6.6)

As indicated in (6.5), \( \Delta V_{DD} \) is the summation of weighted values for \( \Delta V_{THN} \) and \( \Delta V_{THP} \). This is regarded as the process compensation which is accomplished by adding
a fraction of the threshold voltage variations for respective NMOS and PMOS with a proper weight on the supply voltage. Moreover, based on (6.6), D is a function of $\beta_N$ and $\beta_P$. This turns out that the equivalent aspect ratios (W/L) of PMOS and NMOS transistor in the logic gates affect the weight factor D. In this work, the transistors in the logic gates of digital circuits are sized such that D is around 0.5. This is also commonly used in digital circuit design because when D is 0.5, $t_{PLH} \approx t_{PHL}$ which leads to a symmetrical pull down/up performance. Table 6.1 lists the numerical values for the P and N diodes and the calculated weight D using (6.6). It has shown that the calculated D is very close to the simulated value of 0.5, which validates the analysis.

### Table 6.1 Numerical Calculation and Value of Weight D

<table>
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<tr>
<th>Parameters</th>
<th>$\mu C_{ox}$ (μA/V²)</th>
<th>W/L (nm/nm)</th>
<th>$\beta$ (μA/V²)</th>
<th>$\alpha$</th>
<th>$V_{TH}$ (mV)</th>
<th>D</th>
</tr>
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<tr>
<td>NMOS</td>
<td>48.9</td>
<td>720/65</td>
<td>271</td>
<td>1.641</td>
<td>389.1</td>
<td>0.4857</td>
</tr>
<tr>
<td>PMOS</td>
<td>29.04</td>
<td>2160/65</td>
<td>482</td>
<td>2.09</td>
<td>367.2</td>
<td></td>
</tr>
</tbody>
</table>

#### 6.2.1.2. Temperature Variation Compensation

Under temperature variation, the mobility of electrons and holes $\mu(T)$ displays a complementary-to-absolute-temperature (CTAT) characteristic. When the temperature increases, $\beta [=0.5\mu(T)C_{OX}(W/L)]$ decreases. Since the threshold voltage also shows a CTAT characteristic [63], the temperature deviation of $t_d$ in (6.3) is determined by the rate of change in $\beta$ and $V_{TH}$ against temperature for an un-compensated supply (UCS). Of particularly noted, $\Delta V_{THN}$ and $\Delta V_{THP}$ in (6.5) also involve the $V_{TH}$ variation when temperature changes. If the process compensated $\Delta V_{DD}$ is applied to the nominal supply to partially track with the $V_{TH}$ changes as depicted in (6.5), the variation of $t_d$ can be partially compensated when temperature varies. On the other hand, when temperature increases, $\beta_N$ and $\beta_P$ decrease. Meanwhile, the temperature coefficient of
$V_{THN}$ is not equal to that of $V_{THP}$. This leads to different values for $\Delta V_{THP}$ and $\Delta V_{THN}$ across the temperature range. Taken these two effects into account, a temperature compensation error exists in $\Delta V_{DD}$ according to (6.5). Based on the observed temperature behavior in the simulation, $\Delta V_{DD}$ needs to be slightly reduced in order to tackle the temperature compensation error when temperature increases. This is accomplished by injecting a CTAT current into the P and N diodes. As such, when the temperature increases, a temperature-dependent biasing current in the P and N diodes will cause $V_{DD2}$ to be further reduced. This in turn eliminates the temperature compensation error and keeps $t_d$ almost independent of temperature variation.

6.2.1.3. Supply Independency

Refer to Fig. 6.5, the nominal value of supply is decided by the bandgap output voltage $V_{REF}$. After adding the process and temperature compensation voltages, the final supply voltage of digital system is well defined. Due to the power supply rejection (PSR) of the reference block, the DDA and the LDO regulator, the output voltage $V_{DD,C}$ is insensitive to the supply fluctuation. This permits the performance of the digital circuits insensitive to the supply variation.
6.2.2. Circuit Implementation

The PVTCS in Fig. 6.5 is implemented in a UMC 65-nm CMOS process. The detailed circuit topology for each block is discussed as follows.

6.2.2.1. Reference Block and P/N Diodes

Figure 6.6 shows the reference block circuit together with the P and N diodes formed by the transistors MN and MP, respectively. Ria is equal to Rib for i = (2, 3, 5, 6) to achieve a good matching characteristic. To get a reasonable precise VREF, a current-mode bandgap voltage reference topology [54] is utilized. It can provide a low T.C. metric with low supply and low power consumption. The current IREF comprises two parts: I1 and I2. Due to the small T.C. property of VREF and the negative T.C. property of R1−R3, the current I1(T) (∝VREF/(2R3B)) shows a PTAT characteristic. At this juncture, through a voltage-to-current converter formed by the amplifier and R4, I2(T) is generated and its value is equal to VA/R4, where VA is the voltage at node A. Since VA is a CTAT voltage, I2(T) exhibits CTAT characteristic as well. I2(T) is designed to be 3 times of I1(T), the summed current (IREF(T) = I1(T)+I2(T)) flowing into the respective P and N diode retains a CTAT property.

MP and MN are the process and temperature sensing transistors which operate in saturation region on the basis of diode topology. Due to process variation of resistors, I1 and I2 may deviate from their designed values. To alleviate the VGS drift rising from this variation, the aspect ratios of MN and MP are designed to be relatively large. In addition, MN and MP are placed in close vicinity to the target digital circuit in order to accurately sense the process and temperature information.

Figure 6.7 depicts the Monte-Carlo simulation results for VREF/2 and IREF under different temperatures. The results have shown that the reference block can generate a
temperature stable $V_{\text{REF}}$ and a linear CTAT current under process and temperature variations.

Fig. 6.6: Voltage and current reference circuits.

Fig. 6.7 Monte Carlo simulation results for $V_{\text{REF}}/2$ and $I_{\text{REF}}$ under different temperatures.
6.2.2.2. Differential Difference Amplifier (DDA)

DDA is an extension of the op-amp concept dedicated to the multiple floating voltages being forced to equal in a closed-loop feedback circuit [102]. It can be utilized to perform both the addition and subtraction operations. The symbolic as well as the schematic for a 3-port DDA circuit is shown in Fig. 6.8(a) and Fig. 6.8(b), respectively. In this design, the aspect ratio $S(M_{3A}/M_{3B})$ is twice of $S(M_{1A}/M_{1B})$ and $S(M_{2A}/M_{2B})$. Since the bias current is doubled in $M_{3A}/M_{3B}$, the transconductance ($g_m$) of $M_{3A}/M_{3B}$ are two times as that of $M_{2A}/M_{2B}$ and $M_{1A}/M_{1B}$. With this implementation, the final output voltage $V_R$ can be obtained as

$$V_R = \frac{V_{GSN} - V_{REF}}{2} + \frac{V_{GSP} - V_{REF}}{2} + V_{REF}$$

$$\approx \frac{\Delta V_{THN}}{2} + \frac{\Delta V_{THP}}{2} + V_{REF}$$  \hspace{1cm} (6.7)

As revealed in (6.7), the $V_{TH}$ variations ($\Delta V_{THN}$ and $\Delta V_{THP}$) arising from the process and temperature variations are embedded into the normal $V_{REF}$ with the appropriate weights. Since the designed weight for respective $\Delta V_{THN}$ and $\Delta V_{THP}$ is 0.5, we have $S(M_{iA}) = S(M_{iB})$, $S(M_{iC}) = S(M_{iD})$ for $i = (4, 5, 6)$. If a different weight of $\Delta V_{THN}$ and $\Delta V_{THP}$ is required, the current mirror ratio of $S(M_{iA})/S(M_{iB})$ and $S(M_{iC})/S(M_{iD})$ for $i = (4, 5, 6)$ can be changed accordingly.

Figure 6.9 shows the simulated $V_R$ for different $V_{GSN}$ and $V_{SGP}$. $V_{REF}$ is set to be 0.6V. As indicated, the DDA can perform both subtraction and addition functions and generate an accurate $V_R$ based on (6.7).
Fig. 6.8: (a) Symbolic and (b) Schematic of the 3-port differential difference amplifier (DDA).

Fig. 6.9: Simulated $V_R$ under different $V_{GSN}$ and $V_{SGP}$. 
6.2.2.3. LDO Regulator

To drive the digital circuits, a low-dropout (LDO) regulator is employed and depicted in Fig. 6.10. It is based on a simple current-mode feedback buffer structure as the first gain stage whilst using a weighted current feedback (WCF) technique [96]. Through feeding back a weight current to the second gain stage, the WCF can reduce the output impedance to achieve stable operation. Moreover, owing to the low output impedance and the adaptive biasing characteristic for the power transistor driving stage, the regulator has a fast transient response. Due to the point-of-load digital circuit, the minimum $C_L$ in this regulator is designed to be 200 pF and a simple Miller compensation is utilized.

![Diagram of LDO regulator circuit](image)

**Fig. 6.10: LDO regulator circuit.**

Figure 6.11 shows the simulated transient response of the LDO regulator when $I_L$ switches from 1mA to 50 mA in 50ns. As indicated, the LDO regulator displays a
small undershoot and overshoot with fast settling time. Therefore, it is suitable to drive
the fast switching digital circuits.

Fig. 6.11. Simulated transient response for the LDO regulator.
6.2.2.4. Digital Tracked Oscillator

To demonstrate the effectiveness of PVT compensated supply, two digital tracked oscillator blocks are investigated. The first circuit block is a 41-stage inverter chain (Fig. 6.12(a)) to generally model the digital logic gates. The second circuit is a sample critical path (Fig. 6.12(b)) with 45 CMOS logic gates including inverter gates, NAND gates, NOR gates and Transmission gates which are similar to that of the test circuit in [44, 51]. Both circuits are configured as an oscillator. The oscillation frequency is examined under PVT variations. The inverter chain is implemented into silicon to demonstrate the effectiveness of the PVTCS. To ease the measurement, a frequency divider with 64x division is employed to reduce the measured frequency. Extensive simulations of both the inverter chain and the critical path circuit are also conducted.

![Diagram of Digital Tracked Oscillator](image)

Fig. 6.12: Digital load circuits configured as oscillators: (a) Inverter Chain and Critical Path Circuit [27, 60].
6.2.3. Results and Discussions

The microphotograph of proposed circuit is depicted in Fig. 6.13. The active area of the supply system (including the reference block, DDA, and LDO regulator) is 0.1053 mm$^2$. The supply for the reference block and DDA is 1.2 V whilst the supply for LDO regulator is 0.9 V. The total power consumption is 734 µW. To evaluate the improvement factor, the oscillation frequencies from the inverter chain and the critical path using the PVTCS and UCS (nominal value is 0.6 V) are both obtained. The results and discussions are in the subsequent sub–sections as follows.

Fig. 6.13: Microphotograph of the PVT compensated supply system.

6.2.3.1. Results of Inverter Chain

To verify the process variation compensation performance, Monte Carlo (MC) simulations are conducted. The sample size is 500 with 3 sigma (3σ) variation
coverage. Figure 6.14 shows the simulated oscillation frequency distribution of the inverter chain under MC simulations at $T = 27^\circ$. With the PVTCS, the standard deviation ($\sigma$) of the oscillation frequency is reduced by 45.2%.

![Graphs showing inverter chain under PVTCS and UCS simulations](image)

**Fig. 6.14:** Comparison of oscillation frequency of inverter chain under MC simulations when (a) PVTCS and (b) UCS is applied.

Fig. 6.15 compares the simulated oscillation frequency when the temperature changes from -40 to 90 °C. If the total frequency variation across the temperature range (-40 to 90 °C) is defined as $\Delta f = f_{\text{max}} - f_{\text{min}}$, the ratio of $\Delta f$ over the room temperature frequency $f_{\text{mean}}$ ($\Delta f/f_{\text{mean}}$) is obtained. The result has suggested that $\Delta f/f_{\text{mean}}$ is reduced by 91% from the comparison between the PVTCS and UCS.
The measured frequency distribution of 12 chips at room temperature is illustrated in Fig. 6.16(a) for the PVTCS and 6.16(b) for the UCS. Due to the limited samples, the
compensation improvement is smaller than that of the simulated value in Fig. 6.14. However, with PVTCS, the $\sigma$ of the oscillation frequency still shows a 33% reduction.

Figure 6.17(a) and 6.17(b) present the measured $\Delta f/f_{\text{mean}}$ (same definition as that in Fig. 6.15) distribution when the temperature changes from -40 to 90 °C for PVTCS and UCS, respectively. The average value ($\mu$) of $\Delta f/f_{\text{mean}}$ is reduced by 82.9% when the PVTCS is applied.

![Diagram](image)

**Fig. 6.17:** Comparison of oscillation frequency variation of inverter chain under temperature variation for measured 12 chips at (a) PVTCS and (b) UCS.

The test result of supply variation is illustrated in Fig. 6.18. For the PVTCS system, the supply voltages of the reference block, the DDA and the LDO regulator are...
varied by ±5%. Regarding for the UCS performance, the supply voltage of inverter chain is also varied by the same amount. As indicated, the frequency of inverter chain is independent of the supply change for the PVTCS system since the supply voltage of the inverter chain is generated internally by the reference block and DDA. On the contrary, when the UCS increases or decreases by 5%, the frequency is increased or decreased by around 25%. UCS digital circuit is considered quite sensitive to the supply voltage variation.

![Normalized oscillation frequency variation of inverter chain under supply variation for measured 12 chips at PVTCS and UCS.](image)

Fig. 6.18: Normalized oscillation frequency variation of inverter chain under supply variation for measured 12 chips at PVTCS and UCS.

Figure 6.19 depicts the measured waveforms for a single chip under simultaneous temperature and supply variations for both PVTCS and UCS. When the PVTCS is applied, the frequency variation is significantly reduced by 93.8% under temperature and supply variations. Through the built-in frequency divider, the measured frequency values shown in Fig. 6.19 are 1/64 of the actual oscillation frequency of the inverter chain. From the simulation and measured results, it has confirmed that the PVTCS can reduce the frequency deviation of the inverter chain based oscillator under a total of PVT variations.
Fig. 6.19: Measured oscillation waveforms for a single chip under PVTCS and UCS at different input supply and temperature values.
6.2.3.2. Results of Critical Path

The simulated oscillation frequency distribution of critical path under MC simulations at PVTCS and UCS are presented in Fig. 6.20(a) and 6.20(b), respectively. Regarding the input supply variation in case of the PVTCS, $\sigma$ of the frequency is reduced by 42.1%. Regarding the temperature variation, the result is shown in Fig. 6.21. Similar to the inverter chain, the PVTCS can significantly reduce the frequency deviation of the critical path circuit by 87.3% in the temperature range. Finally, when the supply voltage of critical path is decreased or increased by 5% on the basis of nominal value (0.6 V), the frequency of critical path is reduced by 23% or increased by 26%, respectively. It has confirmed that the PVTCS can minimize the speed deviation of the critical path under a total of PVT variations as well.

![Histograms of oscillation frequency distribution](image)

**Fig. 6.20:** Comparison of oscillation frequency of critical path under MC simulations at (a) PVTCS and (b) UCS.
6.2.3.3. Performance Comparison

Table 6.2 summarizes the simulated $\Delta f/f_{\text{mean}}$ for both inverter chain and critical path under worst case in corresponding corner of UCS and PVTCS. As indicated, the PVTCS can significantly reduce the variations of the $\Delta f/f_{\text{mean}}$ in worst case corners. Table 6.3 compares the performance of the proposed PVT compensation supply system with the other reported works. Due to the mismatch of sensing P diode, N diode and the digital circuit transistors, the PVTCS shows reasonable compensation improvement during process variations. However, both the simulation and the measurement results have validated that the PVTCS can reduce the $\sigma$ of oscillation frequency from 30% to 40%. For the temperature compensation, the PVTCS shows better than 80% improvement. Finally, the PVTCS is insensitive to the supply variation which in turn shields the digital circuits from the noisy supplies. Most significantly, due to the simple adaptive supply voltage control mechanism without affecting the body voltage of the digital circuits, the PVTCS system is reliable without encountering the latch-up issue.
### Table 6.2 Performance Improvement of the PVTCS with Respect to the UCS at Worst Cases

<table>
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<th>Parameters</th>
<th>Inverter Chain</th>
<th>Critical Path</th>
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<tbody>
<tr>
<td></td>
<td>PVTCS</td>
<td>UCS</td>
</tr>
<tr>
<td>SS, –40°C, V\text{dd} – 5%</td>
<td>27.2%</td>
<td>79.9%</td>
</tr>
<tr>
<td>FF, 90°C, V\text{dd} + 5%</td>
<td>38.6%</td>
<td>123%</td>
</tr>
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</table>

SS: Slow NMOS Slow PMOS. FF: Fast NMOS Fast PMOS.

### Table 6.3 Performance Comparison with Respect to the Reported PVT Compensation Circuits

<table>
<thead>
<tr>
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<tbody>
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<td>Process (nm)</td>
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<td>130</td>
<td>350</td>
<td>65</td>
<td>65</td>
<td>65</td>
</tr>
<tr>
<td>Power (μW)</td>
<td>NA</td>
<td>N/A</td>
<td>141</td>
<td>N/A</td>
<td>N/A</td>
<td>734</td>
</tr>
<tr>
<td>Body Bias</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Process Var.</td>
<td>85.7%</td>
<td>N/A</td>
<td>71%</td>
<td>82.1%</td>
<td>84.8%</td>
<td>45.2%</td>
</tr>
<tr>
<td>Temperature Var.</td>
<td>N/A</td>
<td>85%</td>
<td>90.4%</td>
<td>N/A</td>
<td>N/A</td>
<td>91%</td>
</tr>
<tr>
<td>Supply Var.</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>22.5%</td>
</tr>
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</table>
6.3. Summary

In this Chapter, the PVT compensation techniques using adaptive body bias and adaptive supply control are firstly reviewed. The limitations and advantages of each method are discussed.

Followed by the review, a point-of-load digital system supply with PVT compensation (PVTCS) is proposed. By adding a weighted combination of the variation of $V_{TH}$ from the P/N transistor diodes on the supply, the delay and the speed of the digital circuits can be kept constant. The operation principle and circuit implementation of each block of the PVTCS are all presented. Validated in a UMC 65-nm process with both inverter chain and critical path digital circuit examples, the simulation and measurement results have demonstrated the PVTCS can minimize the speed deviation of digital circuits under a total of PVT variations. With an on-chip high speed LDO regulator as a supply driver, the PVTCS, which is latch-up free design, is suitable for driving fully on-chip point-of-load digital circuit with PVT compensation.
CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

This Chapter gives the conclusions and future work of this research work.

7.1 Conclusions

This thesis presents a study of threshold monitoring circuits ($V_{TH}$ sensor), wide load capacitance ($C_L$) range output capacitorless LDO (OCL-LDO) regulators and process-voltage-temperature (PVT) compensation techniques for digital circuit systems. All the proposed works are realized in CMOS 65-nm process and analyzed in detail. The results are compared with the representative state-of-the-art works. It turns out the performance metrics of each proposed work meet the design objectives.

The $V_{TH}$ sensor circuits are firstly reviewed. It can generate the $V_{TH}$ of the transistor device at absolute temperature ($V_{TH0}$). Therefore, it can provide the process information. The temperature compensation principle, design constrains under nanometer technologies are discussed. A current-mode second-order temperature compensated $V_{TH}$ sensor is proposed by using the different temperature properties of resistors. It aims to reduce the nonlinear temperature effect of transistor gate-to-source voltage ($V_{GS}$) so as to achieve a low temperature coefficient (T.C.). The results have shown the proposed $V_{TH}$ sensor design achieves a better T.C. with respect to other nanometer voltage reference based designs. It also achieves a comparable T.C. when compared to the $V_{TH}$ sensor circuits which using long channel-length process technologies.
Regarding the LDO regulators, the relevant topologies are discussed. The fundamental understanding of output capacitor (OC) and output capacitorless (OCL) LDO regulators are both presented. The stability and transient performance of each topology are explored in detail. Due to the limitation of driving ability for the conventional frequency compensation techniques, the reported OCL-LDO regulators can only support small $C_L$ range. This raises the motivation to research and investigate new circuit techniques to extend the $C_L$ range driving ability.

Two circuit techniques for OCL-LDO regulator dedicated to drive wide $C_L$ range are proposed. First, a Dual-Summed Miller Frequency Compensation (DSMFC) is employed on a flipped voltage follower (FVF) based regulator circuit architecture. By utilizing an additional simple Miller compensation stage on the basis of Single Miller Compensation (SMC), the non-dominant pole(s) can be pushed to a higher frequency. As such, the stability of regulator under wide $C_L$ range conditions can be achieved. Second, based on a fast-transient multi-gain stage LDO regulator topology, a new weighted current feedback (WCF) technique is proposed. It can dynamically manage the output impedance as well as the gain of the inter-gain stage. With this circuit architecture, the WCF can avoid the right-half-plane (RHP) pole and push the left-half-plane (LHP) non-dominant complex pole pair to a higher frequency. This permits the regulator achieve good stability, high accuracy, fast speed under a wide $C_L$ range. Of particular importance, both proposed wide $C_L$ range LDO regulators achieve good transient figure-of-merit (FOM) with small compensation capacitance.

Finally, compensation techniques to address the performance variations of digital circuits under PVT variations are reviewed and investigated. The adaptive body bias and adaptive supply control are the two typical methods to reduce the PVT variations. Due to the fundamental limitations of body bias for large scale of digital circuits, a
fully on-chip PVT compensated supply (PVTCS) system is thereby proposed. Through adding a weighted combination of $V_{TH}$ variation of PMOS and NMOS transistors onto the normal supply, the speed or delay variations of digital system can be minimized in the context of PVT variations. The WCF technique is also utilized in the regulator design of the PVTCS system.

Overall, the small T.C. $V_{TH}$ sensor, wide $C_L$ range LDO regulators and the PVT compensation supply will be useful for on-chip circuits and systems, particularly for power management system.
7.2 Future Works

The $V_{TH}$ sensor circuit, wide $C_L$ range LDO regulator and PVT compensated supply system have been successfully researched and realized. Although the design objectives of this research work have been met, there are further future research directions that can be investigated.

For the $V_{TH}$ sensor design, low T.C. is achieved by using different type of resistors to construct a second-order temperature compensation. Under process variations, the resistor value may be hard to control, hence trimming is required. This will increase the cost due to the additional T.C. calibration procedure. Based on the limitation, further low T.C. $V_{TH}$ sensor design without temperature trimming can be investigated.

The proposed Type-I and Type-II LDO regulators can drive 10 pF – 10 nF and 470 pF – 10 nF $C_L$ range. Typ-I offers a wider $C_L$ range but a slower response whereas Type-II offers a slightly small $C_L$ range but a faster transient speed. Therefore, a new circuit techniques that can achieve fast transient response and a very wide $C_L$ range, starting from 0 pF, are still in demand.

Besides, digital implementation LDO regulator can be useful due to the continual push from advanced CMOS nanometer technologies. This is mainly because digital implementation is less sensitive to environment disturbances and more robust to the process and temperature variations. It can also works at a lower supply voltage with low quiescent current consumption. This permits the increase of current efficiency of LDO regulator.

Regarding the PVT compensation systems, the proposed PVTCS can reduce the performance variations of digital circuits. However, the improvement factor for process variation is limited due to the mismatch of the P/N diodes and the target digital
circuits. As a result, more precision based process and temperature variation sensor for digital circuit needs to be explored to improve the sensing accuracy.

In addition, the current reference generator in PVTCS is implemented using the bandgap reference circuit and resistors. Due to the variation of resistor values, the generated currents may not be accurately generated, thus degrading the compensation effectiveness. Since the $V_{\text{TH}}$ sensor can generate a PVT insensitive constant current source, the current reference design using the low T.C. $V_{\text{TH}}$ sensor is another research direction.

Finally, to drive the fast transient digital circuit, the LDO regulator has to be fast with high power supply noise rejection. Therefore, high frequency PSR enhancement circuit techniques are desired. The same goes for the $V_{\text{TH}}$ sensor circuit.
AUTHOR’S PUBLICATIONS


REFERENCES


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