IN-CIRCUIT CHARACTERISATION OF DEVICE’S IMPEDANCE FOR SIGNAL INTEGRITY ANALYSIS

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IN-CIRCUIT CHARACTERISATION OF DEVICE’S IMPEDANCE FOR SIGNAL INTEGRITY ANALYSIS

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Statement of Originality

I hereby certify that the content of this thesis is the result of work done by me and has not been submitted for a higher degree to any other University or Institution.

11th November 2011

Date

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Summary

Rapid advances in integrated circuits (ICs) and process technology coupled with surge in consumers’ expectation for powerful processing capabilities and features dramatically change the way for digital circuit designs. With increasing clock speed and shorter rise time, impedance control for interconnects on the printed circuit board (PCB) to ensure good signal integrity (SI) performance has become a critical factor in high-speed digital design. Besides impedance control of interconnects on PCB, it is also equally important to be equipped with the knowledge of input and output impedances of the devices that will be connected to these interconnects. Any slight impedance mismatch will have an impact on the SI performance of the high-speed digital circuit.

To achieve optimal impedance matching at the digital interfaces, one could only rely closely on the recommended equivalent circuit model of the interface from the manufacturer’s datasheet. However, the datasheet is usually suitable for specific application, layout and operating condition. Alternatively, one could utilise circuit simulation together with Input and Output Information Specifications (IBIS) model for input/output (I/O) interface impedance matching, which is straightforward but it provides only an approximate model. For more accurate equivalent interface model, three-dimensional (3D) full-wave modelling tool can be employed but it requires knowledge on the device’s internal details, which is often guarded by proprietary issues.

Based on a two-probe inductive coupling approach, the thesis presents a novel in-circuit measurement method to characterise the impedance of any device (either passive or active) under its actual operating condition. With this in-circuit measurement setup, the impedance of a device can be characterised under intended operating conditions with specifics biasing current, voltage and operating frequency. The accurate and complete electrical characteristic extracted enables proper choice of termination component to achieve optimal SI performance in high-speed digital design with confidence.
Table of Content:

Acknowledgments ........................................................................................................................................... i
Summary ......................................................................................................................................................... ii
List of Figures .................................................................................................................................................... v
List of Tables .................................................................................................................................................... vi
List of Abbreviation and Acronym ................................................................................................................ vii
List of Symbols and Useful constants and Measurement Units ................................................................. vii

1.0 INTRODUCTION .................................................................................................................................... 1
  1.1 Importance of Signal Integrity in High Speed Digital Design ............................................................... 1
    1.1.1 What is Signal Integrity? .................................................................................................................... 1
    1.1.2 Industrial Technologies Trend ........................................................................................................... 2
    1.1.3 Trend in Signal Integrity ..................................................................................................................... 4
    1.1.4 Why Consider Signal Integrity? ........................................................................................................ 5
    1.1.5 Signal Integrity Challenges ............................................................................................................... 6
  1.2 Motivation ................................................................................................................................................... 8
  1.3 Objective and Contributions .................................................................................................................. 10
  1.4 Thesis Organization .................................................................................................................................. 10

2.0 LITERATURE REVIEW ............................................................................................................................... 12
  2.1 High-Speed Digital Design Analysis ...................................................................................................... 12
    2.1.1 PCB Inter-Layer Vias Design .............................................................................................................. 13
    2.1.2 High-speed PCB Interconnects Layout Design .................................................................................... 18
    2.1.3 Crosstalk of PCB Interconnects ......................................................................................................... 28
  2.2 Device Characterization and Modelling ................................................................................................... 31
    2.2.1 Semiconductor Design Model Libraries ............................................................................................ 31
    2.2.2 I/O Buffer Information Specification (IBIS) Model ............................................................................. 33
    2.2.3 Device Characterization through Measurement .................................................................................. 36

3.0 REVIEW OF IMPEDANCE MEASUREMENT .............................................................................................. 44
  3.1 High Frequency Behaviors of Passive Components ............................................................................... 44
    3.1.1 High Frequency Effects on Resistor Characteristic .......................................................................... 45
    3.1.2 High Frequency Effects on Inductor Characteristic ........................................................................... 46
    3.1.3 High Frequency Effects on Capacitor Characteristic ....................................................................... 47
  3.2 Current Measurement ............................................................................................................................... 48
    3.2.1 Advantages of Using Current Probe ................................................................................................ 48
    3.2.2 Measuring Current Signals ................................................................................................................. 48
    3.2.3 Single Probe Measurement Limitation ............................................................................................... 49
  3.3 In-Circuit Measurement using Two Current Probes ............................................................................. 50
### List of Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3.1</td>
<td>High Frequency Current Probe</td>
<td>51</td>
</tr>
<tr>
<td>3.3.2</td>
<td>Injecting Current Signals</td>
<td>51</td>
</tr>
<tr>
<td>3.3.3</td>
<td>Measurement Setup for Optimum High Frequency Performance</td>
<td>52</td>
</tr>
<tr>
<td>3.3.4</td>
<td>Theoretical Background of Two-Probe Measurement</td>
<td>54</td>
</tr>
</tbody>
</table>

### 4.0 VALIDATION OF TWO-PROBE MEASUREMENT METHOD

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1</td>
<td>In-Circuit Characterization of Passive Components</td>
<td>62</td>
</tr>
<tr>
<td>4.2</td>
<td>Measurement Setup for Validation</td>
<td>63</td>
</tr>
<tr>
<td>4.3</td>
<td>Equivalent Circuit of the Test Setup</td>
<td>65</td>
</tr>
<tr>
<td>4.4</td>
<td>Resistor Measurement Results</td>
<td>70</td>
</tr>
<tr>
<td>4.4.1</td>
<td>Nominal Impedance Measurement</td>
<td>70</td>
</tr>
<tr>
<td>4.4.2</td>
<td>Full Frequency Range Impedance Response</td>
<td>71</td>
</tr>
<tr>
<td>4.4.3</td>
<td>Impact of DC Biasing on the Impedance Response</td>
<td>73</td>
</tr>
<tr>
<td>4.5</td>
<td>Inductor Measurement Results</td>
<td>74</td>
</tr>
<tr>
<td>4.5.1</td>
<td>Nominal Inductance Measurement</td>
<td>74</td>
</tr>
<tr>
<td>4.5.2</td>
<td>Full Frequency Range Impedance Response</td>
<td>75</td>
</tr>
<tr>
<td>4.5.3</td>
<td>Impact of DC Biasing on the Impedance Response of the Inductor</td>
<td>76</td>
</tr>
</tbody>
</table>

### 5.0 MEASUREMENT OF ACTIVE DEVICE IMPEDANCE FOR SI ANALYSIS

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>Transmission Line, Reflections and Impedance Matching</td>
<td>78</td>
</tr>
<tr>
<td>5.1.1</td>
<td>Transmission line</td>
<td>78</td>
</tr>
<tr>
<td>5.1.2</td>
<td>Transient Reflections</td>
<td>79</td>
</tr>
<tr>
<td>5.1.3</td>
<td>Lattice Bounce Diagram</td>
<td>82</td>
</tr>
<tr>
<td>5.1.4</td>
<td>Impedance Matching Technique</td>
<td>84</td>
</tr>
<tr>
<td>5.1.5</td>
<td>Challenges in Source Matching</td>
<td>89</td>
</tr>
<tr>
<td>5.2</td>
<td>Measurement of Output Impedance of Clock Driver</td>
<td>90</td>
</tr>
<tr>
<td>5.3</td>
<td>Case Study on Series Termination Selection</td>
<td>92</td>
</tr>
<tr>
<td>5.4</td>
<td>Clock Driver Circuit for Case Study</td>
<td>93</td>
</tr>
<tr>
<td>5.5</td>
<td>Extraction of Clock Driver Output Impedance</td>
<td>96</td>
</tr>
<tr>
<td>5.6</td>
<td>Clock Driver Output Impedance Measurement Results</td>
<td>99</td>
</tr>
<tr>
<td>5.7</td>
<td>Validation with Simulation Results</td>
<td>106</td>
</tr>
<tr>
<td>5.8</td>
<td>Experimental Validation with Measurement Results</td>
<td>108</td>
</tr>
<tr>
<td>5.9</td>
<td>Impact of Series Termination on Rise-time and Emission</td>
<td>110</td>
</tr>
</tbody>
</table>

### 6.0 CONCLUSION

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>Major Contribution of the Thesis</td>
<td>112</td>
</tr>
<tr>
<td>6.2</td>
<td>Limitations and Recommended Future Research Work</td>
<td>114</td>
</tr>
</tbody>
</table>

Author’s Publications ........................................................................ 116
Bibliography ..................................................................................... 118
Author’s Biography .......................................................................... 128
Appendix A: List of EDA Vendors and Tools ...................................... 129
List of Figures:

Figure 1 : Trend in process technology ................................................................. 2
Figure 2 : Trend in cycle time reduction: processor/speed/gate density trend ........... 3
Figure 3 : Design cost structure relationship .......................................................... 5
Figure 4 : High speed digital signal integrity challenges ..................................... 7
Figure 5 : (a) Typical through hole via structure and (b) common types of vias ....... 13
Figure 6 : Via diameter analysis (a) via structure and parameter setup, (b) TDR response, (c) $S_{21}$ insertion loss response and (d) $S_{11}$ reflection loss response [21] ............ 14
Figure 7 : Via height analysis (a) via structure and parameter setup, (b) TDR response, (c) $S_{21}$ insertion loss response and (d) $S_{11}$ reflection loss response [21] ............ 15
Figure 8 : $S_{21}$ improvement for via with and without stub [21] .......................... 16
Figure 9 : Improved $S_{21}$ performance by back drilling (from Sanmina-Sci) [111] ....... 16
Figure 10 : Case study on via effect on SI (a) test structure, (b) TDR response, (c) $S_{11}$ reflection loss and (d) $S_{21}$ insertion loss response. [21] ......................... 17
Figure 11 : Example of industry impedance solver and layout stackup .................. 18
Figure 12 : TDR impedance measurement of a PCB trace using Agilent TDR system ..., 19
Figure 13 : AC resistive losses in the cross sectional view of the conductor wire [39] .... 20
Figure 14 : Cross sectional illustration of a typical PCB surface roughness [39] ....... 21
Figure 15 : Loss tangent of some common substrate material [41] ......................... 22
Figure 16 : Typical trace bend structures configurations ........................................ 23
Figure 17 : Effects of TDR response of various bend structures ......................... 24
Figure 18 : Surface current simulation plot (a) right angle (b) round bend ............ 24
Figure 19 : Near-Field emission plot (a) right angle bend (b) round bend ............ 24
Figure 20 : Two conductors microstrip interconnects over common return plane .... 25
Figure 21 : Interconnects transverse over different return planes ....................... 26
Figure 22 : Surface current plot for (a) without and (b) with one ground return via design ................................................................. 26
Figure 23 : Ground return via design (a) 4 ground vias and (b) single ground via ....... 27
Figure 24 : TDR response of one ground return via design configuration .......... 27
Figure 25 : $S_{21}$ response of one ground return via design configuration .......... 27
Figure 26 : Microstrip FR-4 test structure for crosstalk simulation and measurement (a) electric and magnetic fields and (b) equivalent circuits of two parallel lines. 28
Figure 27 : Microstrip FR-4 test structure for crosstalk simulation and measurement .... 29
Figure 28 : Crosstalk validation (a) simulation results and (b) measurements .. 29
Figure 29 : Overall effects of trace separation for microstrip (a) NEXT and (b) FEXT ... 30
Figure 30 : Overall effects of trace separation for microstrip (a) NEXT and (b) FEXT ... 30
Figure 31 : Typical IBIS model, input and output structure ................................ 34
Figure 32 : Measurement techniques and frequency range[76] .............................. 36
List of Tables

Figure 33: Bridge measurement method ................................................................. 37
Figure 34: I-V measurement method ..................................................................... 38
Figure 35: Resonant or roll-off measurement method ........................................... 39
Figure 36: Auto balancing bridge measurement method ...................................... 40
Figure 37: Network analysis measurement method and sensitivity comparison [76] 41
Figure 38: RF I-V measurement method [76] ....................................................... 42
Figure 39: Equivalent circuit of a non ideal resistor [80] ...................................... 45
Figure 40: Characteristic response (a) a 500 Ω thin-film resistor and (b) metal-film with difference values [81] ............................................................ 45
Figure 41: Equivalent circuit of a non ideal inductor [80,81] ............................... 46
Figure 42: Characteristic response of an inductor [81] ........................................ 46
Figure 43: Equivalent circuit of a non ideal capacitor [80] ................................. 47
Figure 44: Characteristic response of a capacitor [81] ......................................... 47
Figure 45: CT6 probe frequency response [78] ....................................................... 52
Figure 46: CT6 positioning for HF application [79] .............................................. 53
Figure 47: (a) Basic test setup; (b) equivalent circuit of two probes measurement ... 54
Figure 48: Equivalent circuit of the injection probe .............................................. 55
Figure 49: Reflected equivalent circuit of injection probe in CUT loop ............... 56
Figure 50: Final reflected equivalent circuit of the two probes measurement ...... 57
Figure 51: Measurement setup using the two inductive coupling probes: (a) schematic circuit (b) fabricated test jig .................................................... 64
Figure 52: Equivalent circuit for the in-circuit measurement setup ....................... 65
Figure 53: Simplified equivalent circuit for the measurement setup .................... 67
Figure 54: Magnitude of Zset up versus frequency ............................................. 68
Figure 55: Magnitude of k versus frequency ....................................................... 69
Figure 56: Impedance profile characterisation validation (a) propose two probe test setup and (b) instrumentation setup using Impedance analyzer ...... 71
Figure 57: Comparison of impedance versus frequency (a) 30 Ω and (b) 220 Ω resistor 72
Figure 58: Impedance versus frequency of a 220 Ω resistor under various biasing conditions (0 mA, 5 mA and 15 mA) ................................................ 73
Figure 59: Comparison of impedance versus frequency of a 2.2 μH inductor .......... 75
Figure 60: Impedance versus frequency of an inductor under various biasing conditions (0 mA, 5 mA and 15 mA): (a) 250 μH (b) 47 μH ......................... 77
Figure 61: A 10MHz clock signal measured at a mismatch transmission trace ....... 79
Figure 62:典型信号源，通过传输线驱动一个接收器 ................................. 80
Figure 63: Lattice diagram illustrating the effects of signal multiple reflections ......... 82
Figure 64: Simulated signal at the receiver at the far end of the transmission load side using 2ns rise-time without termination ............................... 83
Figure 65: Simulated signal at the receiver at the far end of the transmission load side using 0.1ns rise-time without termination ........................................ 83
List of Tables:

Table 1: Comparison of measured impedance of resistors at 1 MHz ......................... 70
Table 2: Comparison of measured impedance of inductors at 2 MHz* ....................... 74
# List of Abbreviations:

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>BGA</td>
<td>Ball Grid Array</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Rate</td>
</tr>
<tr>
<td>CAE</td>
<td>Computer Aided Engineering</td>
</tr>
<tr>
<td>CE</td>
<td>Compromising emanations</td>
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<tr>
<td>CISPR</td>
<td>International Special Committee on Radio Interference</td>
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<tr>
<td>CM</td>
<td>Common Mode</td>
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<tr>
<td>COTs</td>
<td>Commercial Off-the-Shelf</td>
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<tr>
<td>CST</td>
<td>Computer Simulation Technologies</td>
</tr>
<tr>
<td>CUT</td>
<td>Circuit Under Test</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
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<tr>
<td>DM</td>
<td>Differential Mode</td>
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<tr>
<td>EDA</td>
<td>Electronic Design Automation</td>
</tr>
<tr>
<td>EM</td>
<td>Electromagnetic</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
</tr>
<tr>
<td>ESL</td>
<td>Equivalent Series Inductance</td>
</tr>
<tr>
<td>FCC</td>
<td>Federal Communications Commissions, USA</td>
</tr>
<tr>
<td>FDTD</td>
<td>Finite Difference Time Domain</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite Element Method</td>
</tr>
<tr>
<td>FEXT</td>
<td>Far End Crosstalk</td>
</tr>
<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
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<tr>
<td>IO</td>
<td>Input/Output</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
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<td>IBIS</td>
<td>Input/Output Buffer Information Specification</td>
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<td>NEXT</td>
<td>Near End Crosstalk</td>
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<tr>
<td>OATS</td>
<td>Open Area Test Site</td>
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<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PUL</td>
<td>Per Unit Length</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RE</td>
<td>Radiated Emission</td>
</tr>
<tr>
<td>2D</td>
<td>Two-Dimensional</td>
</tr>
<tr>
<td>3D</td>
<td>Three-Dimensional</td>
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<tr>
<td>SPICE</td>
<td>Simulation Program with Integrated Circuit Emphasis</td>
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<tr>
<td>VNA</td>
<td>Vector Network Analyzer</td>
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<td>SA</td>
<td>Spectrum Analyzer</td>
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<td>SMT</td>
<td>Surface Mount Technology</td>
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<tr>
<td>SMD</td>
<td>Surface Mount Device</td>
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<tr>
<td>SI</td>
<td>Signal Integrity</td>
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<tr>
<td>TBD</td>
<td>To Be Defined/Determined</td>
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<tr>
<td>TDR</td>
<td>Time Domain Reflectometer</td>
</tr>
</tbody>
</table>
List of Symbols

$\omega$  Angular frequency
$\Omega$  Resistance ohms
$Q$  Quality factor or Q-factor
$f_{\text{res}}$  Resonant frequency
$R_s$  Series Resistance
$Z_x$  Impedance of x
$Z_o$  Characteristic Impedance
$Z_{\text{DUT}}$  Impedance of Device Under Test
$M_x$  Mutual inductances of circuit x
$X_L$  Inductive Reactance
$X_c$  Capacitive Reactance
$\varepsilon_r$  Relative Permittivity of material $= 4$
  (for typical FR-4 unless otherwise specified)
$\varepsilon_0$  Permittivity of free space $= 8.854 \times 10^{-12} \text{ F/m}$
$\mu_0$  Permeability of free space $= 4 \pi \times 10^{-7} \text{ H/m}$
$c$  Speed of electromagnetic waves in free space $\approx 3 \times 10^8 \text{ m/s}$

List of Measurement units

mA  Current  milli Ampere
mV  Voltage  milli Volt
$\mu$H  Inductance  micro Henry
nH  Inductance  nano Henry
$\mu$F  Capacitance  micro Farad
pF  Capacitance  pico Farad
k$\Omega$  Resistance  kilo ohms
mm  Length  milli meter
$\mu$m  Length  micro meter or micron
ns  Time  nano second
ps  Time  pico second
GHz  Frequency  Giga-Hertz
MHz  Frequency  Mega-Hertz
kHz  Frequency  kilo-Hertz
1.0 INTRODUCTION

1.1 Importance of Signal Integrity in High Speed Digital Design

1.1.1 What is Signal Integrity?

“Signal Integrity” [1, 2] is a high-speed design practice that ensures the transmitted signals are received correctly at the receiver. In physical design, it is about meeting voltage and timing specifications to prevent circuit failure and intermittent errors.

Signal Integrity is a field of study involving not only high-speed digital design but also analogue design with operating frequency overlapping into the radio frequency (RF) design arena. It is about signal waveform quality, signal coupling, power distribution network and electromagnetic interference (EMI) compliance to ensure proper functioning of the high-speed design.

Quote from Dr. Howard Johnson, a leading expert on signal integrity:

"Signal Integrity is not just a "nice to know" subject, it is a deterministic, predictable field of study, a "hard science" so as to maximize the performance and minimize the cost of interconnection technology used in high-speed digital designs. It’s all about how to build really fast digital hardware that really works.”
1.1.2 Industrial Technologies Trend

Just in the last decade, the data rates and device’s speed have already pushed the digital design to a new era into the RF arena. On-chip speed is now commonly over 500 MHz and board buses speed including the onboard interface signals are well above 500 MHz into the GHz range. These changes can be seen in the trend presented in Fig. 1.

![Trend in Process Technology](image)

*Figure information are compiled based on data from literature survey, various suppliers and manufacturers’ websites and data sheets.*
Fig. 2 further illustrates the progress of some of the commonly used products in the market. It shows the continuing trends in the following three areas that affect high-speed circuit design:

- Reduction in cycle time;
- Increase in processor operating speed; and
- Increase in gate density.

![Processor-Speed/Gate Density Trend](image)

**Figure 2:** Trend in cycle time reduction: processor/speed/gate density trend*

* Figure information are compiled based on data from literature survey, various suppliers and manufacturers' websites and data sheets.
1.1.3 Trend in Signal Integrity

Signal Integrity (SI) was almost none existence even during the late 80’s as device operating speeds were in the order of 10-20MHz. Entering the late 90’s, device operating speeds were increasing faster than the designer expected and problems of SI began to surface, resulting in signal degradation and even malfunctioning of the circuits. These design challenges and problems related to SI will be discussed in greater details in section 1.1.5. The topic of SI [8, 9] that was once considered good to have, now has been brought back to the front stage and more recently has become one of the most important design issues in the high-speed digital design. A major consideration for all product designers for high-speed digital devices which were once available to the high-end users but now abundantly found in most consumer electronics. The historical development of the device technology and SI design methodologies are briefly summarised as follows:

70’s: Introduction of 7400 class of TTL devices, Bipolar and CMOS and ECL combinational and asynchronous design, operating in several MHz with 5 ns edge rate. Practically, there was no SI issue.

80’s: Introduction of high-speed CMOS and open drain buses, operating speeds at 10 MHz with 2-3 ns edge rate. SI began to surface for long printed circuit interconnects.

90’s: SSTL, AGTL, open collector bus, low voltage devices with edge rate <1 ns were introduced. High-speed differential signalling and synchronous design emerged. Advanced PC’s (486 66MHz, 200 MHz and 350 MHz) with affordable prices were available. IBIS was introduced and well accepted. Extensive circuit timing simulation was necessary.

00’s: GHz clock operation with edge rate <500 ps. High-speed serial interface has taken over parallel bus. USB2.0, SATA, PCI express, Gbps Ethernet and SRIO emerge. SI has become a necessity in digital design with extensive simulation using 2.5D/3D field solvers together with comprehensive TDR and VNA measurements for SI analysis, impedance control and extensive termination techniques to minimise reflection and EMI.
1.1.4 Why Consider Signal Integrity?

Fig. 3 gives a clear illustration of the relationship between various design phases and availability of solution techniques, investment cost and cost of rectification due to failure. It clearly shows that as design requirement, complexity and speed increases, and to minimise the cost of product, the optimum choice has shifted down to the design phase over the years. Fixing problems in the production phase is no longer acceptable as it is extremely costly to rectify, less effective and very often no solution exists except to re-design, which causes delay in product launch and significant increase in product development cost. Hence, addressing SI too late at the design phase will incur significant product development cost.

Figure 3: Design cost structure relationship

* Was derived with Information taken from (1)Edward K.Chan, Mauro Lai, Myoung Hoon Choi, Woong Hwan Ryu, Intel Corps “Concurrent Analysis of Signal-Power Integrity and EMC for high Speed Signaling systems”, EMC 2007, (2) Intel Higher Education, class1 by Richard Mellitz “Signal Integrity Introduction” as well as (3) from author’s company past data
1.1.5 **Signal Integrity Challenges**

The continuous rapid advancement in technologies coupled with an increasing demands in high-tech consumer products that are powerful, compact and cost effective for the consumers; has a direct impact on the design that challenges the ability to deliver products faster, better and reliable. This translates to a very challenging board design requirement, which includes:

- Compact and complex board layout requirement;
- Accurate modelling and simulation to ensure one time success cycle;
- Advance SI design platform for overall performance analysis; and
- Accurate high-speed measurement and design validation.

SI issues occur whenever the signal becomes distorted or the signal to noise ratio starts to degrade. As the operating frequency increases, non-ideal effects of PCB traces cannot be ignored. Some of the challenges faces by designers include:

- Rise time degradation, inter-symbol interference and collapse of eye pattern.
- Electromagnetic coupling, crosstalk and EMI radiation effects.
- Degradation of signal performance due to impedance discontinuities from via, connectors and even signal traces and terminations.

With ever-increasing device speeds, we have reached a point where we must change the way digital products is designed. High-speed design considerations such as issues mentioned above have become highly challenging tasks. Advance SI analysis techniques and tools coupled with in-depth design modelling and simulation to analyse the effects accurately has become a necessity to ensure good design success rate within the tight design schedule. Problems in high-speed digital design are very complex, as shown in Fig. 4.
Figure 4: High speed digital signal integrity challenges
1.2 Motivation

Most high-speed design engineers rely heavily on design guidelines given in the so-called “well-established standards” that were passed down from experienced engineers. These guidelines are usually based upon sound engineering judgments, past experiences and general rules of thumb with little rigorous analyses supporting them. These techniques worked in the past as clock speeds were relatively low and timing margins were large but no longer sufficient and suitable in today’s high-speed design.

With the trends of increasing operating frequency, edge rate and PCB packing density, much research work [1-5] has been carried out in the area of SI. Extensive work has been reported in literature on the interconnect-related aspects, such as mismatches due to discontinuities in inter-layer transitions, interconnects modelling and non-ideal ground effect. Due to the demands in SI analyses, advanced EDA and EM solvers have also been developed in the industries for examples; Cadence, Ansoft, Agilent EEsof, CST, just to name a few. A comprehensive list can be found in Appendix A. Besides interconnects, the information on device’s input and output impedance are also crucial for SI design. Some work has been reported on the device’s input and output interface impedances [82-89] which will be discussed in the literature review in section 3.3. In order to accurately and confidently design high-speed circuit to meet stringent SI requirement for optimised performance. The following key parameters are to be considered in SI design and analysis:

- Access to accurate information of IC’s output Impedance;
- Selection of appropriate termination for impedance matching;
- Accurate design of PCB interconnects for impedance control; and
- Overall design evaluation platform for performance analysis.

A lot of research work has been carried out in interconnect designs and very little has been reported on the IC’s output impedance extraction. Hence, the focus of this thesis will be on the technique to extract the output impedance information of a device for SI design purposes. Off-circuit measurement is commonly adopted by manufacturers
to characterize the impedance behaviour of a passive component for a specific frequency range. The measured impedance serves well for most design purposes. However, it is not suitable for passive components that exhibit non-linear behaviours (e.g. inductors with ferrite cores) and active components where their impedance behaviours vary due to factors such as biasing condition and load current.

With the constraints of off-circuit measurement, the motivation of this thesis is to develop and validate an in-circuit measurement technique that allows the extraction of a device’s output impedance characteristic over a wide frequency range under its intended operating conditions. The extracted impedance information allows the designer to optimise SI performance through proper selection of termination components for impedance matching purposes, which is crucial in high-speed digital design. In-circuit measurement emulates the actual operating condition of the active device and allows the output impedance of the device be extracted with confidence. The proposed two-probe in-circuit measurement approach with careful calibration process to eliminate measurement setup error has demonstrated its accuracy to extract in-circuit impedance up to the GHz frequency range.
1.3 Objective and Contributions

The main objective of this thesis is to explore an in-circuit measurement method to extract a device’s impedance with reasonable accuracy for SI design purposes. A two current probes measurement technique is proposed so that it allows in-circuit measurement of a device’s impedance over a wide frequency range up to 1 GHz. The proposed measurement approach has been first validated in the characterization of passive components up to 1 GHz under in-circuit operation. Then the technique is extended to the characterization of output impedance of an active high-speed clock driver. The results of the output impedance information extracted have been shown to be accurate up to 1 GHz. Finally, these results obtained have been found to be useful with a practical high-speed clock circuit design example.

1.4 Thesis Organization

This chapter gives an overview of SI and the relevant background. The motivation, focus and objective of the thesis are also described. The remaining chapters of the thesis are organised as follows:

Chapter 2 provides a comprehensive literature review of SI related topics such as high-speed digital design analysis, EM field solver and EDA tools, methodology in SI solution as well as the importance of impedance control and interconnects design. It also covers a review of existing device characterisation, modelling tools and measurement instrumentation for SI performance analysis.

Chapter 3 reviews the fundamentals of impedance measurement and describes the theoretical background of single current probe measurement technique. The two current probes in-circuit measurement technique is proposed and the pre-measurement procedure to eliminate possible error due to the measurement setup is described.
Chapter 4 validates the proposed two current probes measurement approach described in Chapter 3. Using passive components such as resistors and inductors under specific biasing conditions as test cases, the measured results using the proposed approach are compared with those obtained from impedance analyser. The ability of the proposed approached to detect the effects of biasing current on the impedance characteristic of the inductors are also demonstrated.

Chapter 5 extends the proposed two current probes approach to measure the output impedance of active devices. The high-speed clock drivers are used as test cases to demonstrate how their output impedances under actual operating conditions are extracted. The extracted impedance is then used for the validation and analysis on proper selection of series termination resistor to achieve optimised SI, rise-time and EMI emission performances.

Chapter 6 concludes the contributions of the thesis and addresses the limitation of the proposed measurement technique. Finally, some possible future work that is worth exploring is recommended.
2.0 LITERATURE REVIEW

As operating speed increases, the electronic system’s electrical performance is no longer determined only by the ICs but also influenced significantly by metal interconnects on the PCB where these ICs are mounted. As timing budget reduces because of higher operating speed, it increases the timing uncertainty of the digital signal as it arrives at the receiving end of the interconnecting trace. Hence, transmission line effects and signal quality due to IC-interconnect interface that could be neglected in the past can no longer be ignored and must be accounted for in high-speed digital design. In order to predict high frequency effects with good accuracy, fine details of interconnects layouts have to be properly modelled so that the impedance of interconnects, IC’s output impedance and the terminations can be well characterised for impedance matching to ensure optimised SI performance.

2.1 High-Speed Digital Design Analysis

In today’s high-speed digital design, designers are resorting to using sophisticated modelling tools, such as 3D full-wave EM field solvers* to accurately model, simulate and analyze the electrical performance of the signal propagating on interconnect structures. In the last decade, there has been extensive research work in high-speed digital designs, such as via design and modelling, PCB trace layout design and consideration, ground return vias and crosstalk analysis, etc. An overview of the interconnect-related research will be summarised in this section.

* 3D refers to a 3 dimensional geometry based classification of Electromagnetic field solvers which are specialized software that solve (a subset of) Maxwell's equations directly.
2.1.1 PCB Inter-Layer Vias Design

In high-speed digital design, every slightest discontinuity on the board has to be considered carefully, especially the vias, which are abundantly used in digital design. With signal rise time reduces, impedance discontinuity due to via results in signal reflections and hence, deterioration of SI and system performance. Therefore, the effect of via in high-speed PCB design poises tremendous challenges to the designer and can no longer be ignored. The usual design practices using rules of thumb or past parameters setting are no longer sufficient. Instead a clear understanding of the impact of the mechanical design of a via on the SI performance is important.

A typical via structure is shown in Fig. 5(a) and the various common types of via used in PCB design are shown in Fig. 5(b).

![Diagram of Typical Through Hole Via and Common Types of Vias](image)

Figure 5: (a) Typical through hole via structure and (b) common types of vias

There has been extensive research in the electrical model extractions of via structures [10-13], effects of via transition performance analysis and characterisation [14-18], advanced via structure for high-speed applications [19] and even impedance controlled via design [20]. Through hole vias are by far is still and will continue to be the most commonly used in the industry simply because of its ease of manufacturing and low-cost. Looking at the via structure, clearly the via diameter, via height and via stub in a through hole via are crucial parameters of via design [21].
a) Effects of Via Diameter Variation

PCB designers choose via diameter based on suppliers/manufacturers preferred recommendation, which is determined by their confidence and process capability and often with high reliability and high yield. This can range conservatively from 0.1 - 0.9 mm as indicated in Fig. 6(a). It is found that for practical high-speed design, impedance variation should be kept within 10% tolerance. For 50 Ω characteristic impedance, the tolerance will be ±5 Ω. Fig. 6(b) shows that via diameter should not be larger than 0.3 mm so as to yield an insertion loss ($S_{21}$) of less than 0.5 dB and a reflection loss ($S_{11}$) of at least 10 dB, as shown in Fig. 6(c) and Fig. 6(d), respectively.

![Image of via diameter analysis](image)

Figure 6: Via diameter analysis (a) via structure and parameter setup, (b) TDR response, (c) $S_{21}$ insertion loss response and (d) $S_{11}$ reflection loss response [21]
b) **Effects of Via Height Variation**

Height is another primary factor that influences the inductance of a via. Depending on the design complexity, the number of layers of the PCB varies, and hence the overall PCB thickness. The height of the through hole via is determined by the overall thickness of the PCB. Typical high-speed PCB thickness ranges from 1.0 mm to 1.8 mm. For more complex designs and military applications, the PCB thickness can go above 3 mm.

![Image of via height analysis and parameter setup](image)

**Figure 7**: Via height analysis (a) via structure and parameter setup, (b) TDR response, (c) $S_{21}$ insertion loss response and (d) $S_{11}$ reflection loss response [21]

From the simulation results shown in Fig. 7, the thicker the board (the longer the via height), the higher the impedance variation during signal transition and leading to higher insertion loss and lower reflection loss. For optimal performance, via height should be kept within 1.5 mm in order to keep impedance variation within 10% tolerance. This would yield an insertion loss ($S_{21}$) of less than 0.5 dB and reflection loss ($S_{11}$) greater than 10 dB.
c) Effects of Excess Via Stub

In high-speed board design utilizing through hole vias, when a signal moves from a top layer to an internal strip line structure, a dangling or excess via stub is created as shown in Fig. 8. Depending of the signal speed and stub length, the signal performance may be compromised. The designers have to decide tradeoffs between cost (using blind via) and performance.

![Figure 8: S21 improvement for via with and without stub][21]

Fig. 8 shows the insertion loss ($S_{21}$) of the via with stub length varying from 0.5 to 3 mm. The capacitance resulted from the excess via stub causes a resonance with the via inductance. The longer the excess stub results in larger capacitance and hence, leads to a lower resonant frequency. Such resonance is undesirable as it increases the insertion loss significantly near the resonant frequency. Typical PCB thickness or via height less than 2 mm will allows an operation bandwidth ($S_{21} < 3$ dB) in excess of 10 GHz. Fig. 9 shows an illustration of using buried via by back drilling and the improvement in $S_{21}$.

![Figure 9: Improved S21 performance by back drilling (from Sanmina-Sci)][111]
d) Effects of Vias Design on SI Performance

To demonstrate the effects of well-designed vias against a typical via design, a 60 mm trace transits between a 4 layer FR-4 PCB ($\varepsilon_r = 4$, Trace width = 6mil, 50 $\Omega$) using two different sets of vias design parameters was studied. Set A has a via height of 1.3 mm and a via diameter of 0.2 mm while Set B has a via height of 2.8 mm and a via diameter of 0.5 mm.

The 60 mm stripline structure in Fig. 10(a) shows two vias transitions. Set A has a much better TDR impedance response with less impedance fluctuation hence leading to wider operating bandwidth and lower insertion loss as observed in Fig. 10(b-d). This case study clearly shows the importance of via design on high-speed PCB layout. The seemingly small changes in the via design can affect the impedance mismatch significantly and degrades the signal propagation performance.
2.1.2 High-speed PCB Interconnects Layout Design

For high-speed applications where signal rise time is in the range of sub nano-second region, it translates into a signal bandwidth of more than 1 GHz, overlapping into the RF or microwave region. At these frequencies, the PCB metal interconnects whose physical length becomes comparable to the signal wavelength begins to exhibit transmission line effects [22, 23]. Also, a poorly designed trace without ground return via will cause significant impedance discontinuity, leading to degradation of SI performance. Much work has been reported in the areas of high-speed interconnects modelling and analysis [24-38] for high-speed interconnects designs. The reported work will be briefly summarised in this section.

a) Importance of Trace Stackup and Trace Impedance

In today’s high-speed layout design, impedance control becomes a primary issue and its effect has to be considered seriously. The design of interconnect trace impedance on the PCB is dependent on the trace dimension, layer stackup and material used. Many industry design tools based on the mathematical formulation are available to assist designer today in the PCB design such as Polar Si8000 Quick Solver and Speedstack*. Fig. 11 shows how these tools allow designer to optimise the PCB stack up design for desire trace’s characteristic impedance.

However, even with the presence of state of art simulation tool in the stackup design, due to fabrication deviations, the actual trace impedance is often deviated from the desired value. With existing accuracy in the PCB fabrication process, 20% is an industrial acceptable norm while 10% is considered a stringent specification.

Hence, actual trace impedance has to be well characterised in order to ensure impedance matching on actual PCB termination design to ensure optimise SI, which is crucial in high-speed digital design. One such tool that is extremely critical and essential is the time domain reflectometer (TDR) that is very useful for fast, accurate and reliable PCB impedance characterization as shown in Fig. 12. Its key role is to validate the actual PCB structure characteristic, to create an equivalent model for SI analysis and simulation.

![Figure 12: TDR impedance measurement of a PCB trace using Agilent TDR system](image)

*Agilent application note, "SI Analysis series, part1: single Port TDR, TDR/TDT and 2-Port TDR”, 5989-5763ED Feb. 2007
b) **Non Ideal Interconnect Losses**

With lower operating speeds, PCB traces can be approximated as perfect conductors (usually defined as Perfect Electrical Conductor-PEC in EM simulation) with their losses ignored. As more designs are operating in very high-speed application not only the transmission lines characteristics are critical but also other non-ideal effects [39, 40]. These effects become significant in high-speed design as they affect the signal propagation behaviour on the interconnects. There are many conventional formulas that are available to determine the characteristic impedance and propagation delay for lossless transmission line model. However, as frequency increases into the GHz range, the following losses of the interconnects can no longer be ignored:

**(i) AC Resistive Losses**

At low frequency, current density within the conductor is uniform across the cross sectional area of the conductor. The resistance is given by:

\[
R_{dc} = \frac{\rho L}{A_{outer - inner}} = \frac{\rho L}{wt}
\]

where \(\rho\) is resistivity of the conductor, \(L\) is the length of the conductor and \(A\) is the cross-sectional area. For a PCB trace, \(w\) is the trace width and \(t\) is the trace thickness. As frequency increases, the current tends to migrate towards the outer surface as shown in Fig. 13, commonly known as the “skin effect”. It causes the current to flow in a smaller area than the case of lower frequency. Hence, the effective resistance increases with frequency.

![Coaxial Cable Cross Section at High Frequency](image)

**Figure 13:** AC resistive losses in the cross sectional view of the conductor wire [39]
(ii) Surface Roughness

In the standard transmission line model evaluation, it usually assumes a perfectly smooth surface, which again in reality is never true. All metal interconnect surface are rough under microscopic view as shown in Fig. 14. They are controlled in order to have good adhesion to the laminate in the PCB formation.

![Cross sectional illustration of a typical PCB surface roughness](image)

Figure 14: Cross sectional illustration of a typical PCB surface roughness [39]

As frequency increases high enough (~200 MHz), current tend to travel on the outer skin surface due to skin effect and with skin depth approaches the tooth size of copper. (Typical FR-4 boards has a average tooth size of 4-7 µm) Hence, the tooth like surface roughness has to be taken into consideration, which increases the effective path length and decreases the area. The roughness can increase the AC resistance by 10-50% and is also frequency dependent. However, as the geometric tooth structure is random in nature, the loss associated with surface roughness can be difficult to predict.

(iii) Dielectric Losses

In most cases, dielectric losses can be ignored because the conductor losses are more dominant. However, as frequency increases, this is no longer true. When a time varying electric field is impressed on a material, any molecules in the material that are polar in nature will tend to align in the direction opposite that of the applied field. Permittivity is the measure of how the electric field is affected by the dielectric medium. This relates to the material ability to transmit an electric field.
Permittivity of a dielectric medium is given by:

\[ \varepsilon = \varepsilon' - j\varepsilon'' \]  

The real part of the permittivity is given by:

\[ \varepsilon' = \varepsilon_0 \varepsilon_r \]  

where \( \varepsilon_0 \) and \( \varepsilon_r \) are the permittivity of free space and relative permittivity of the dielectric material, respectively. The imaginary part \( \varepsilon'' \) represents the loss which is proportional to frequency. The real and imaginary parts are related by the “loss tangent” or \( \tan \delta \) defined as follows:

\[ \tan \delta = \frac{\varepsilon''}{\varepsilon'} \]  

The loss tangents of some typical substrate materials are given in Fig. 15.

Figure 15: Loss tangent of some common substrate material [41]
c) Effects of Trace Bends on Signal Performance

In almost all PCB designs, signal trace routing involves some form of bends to allow the trace to avoid obstacles, such as vias and components. Much research has been done on modelling and analyzing trace bends [42-45]. When a signal on an interconnect encounters a bend, impedance discontinuity occurs and causes reflection of the signal. For thin traces at low speed, this poise negligible effects and if needed, simple lumped capacitance model [40] is usually adequate to model the effect of the bend. However, in high-speed design with space constraints, multiple bends are commonly needed and their effects simply cannot be ignored. Some design issues dealing with trace bend are the effects on SI and the operating bandwidth.

Fig. 16 shows some possible bend structures in high-speed layout design,

![Figure 16: Typical trace bend structures configurations](image_url)

The effect of a bend can be clearly seen in the TDR response as shown in Fig. 17 and the surface current using the CST-MWS simulation as shown in Fig. 18 [46]. Fig. 18 clearly shows that there is a current density build-up at the inner corner for the sharp 90° bend. Such an effect is negligible for the case of rounded bend. Similarly, the measured near-field emission pattern using the Langer IC Scanner (FLS-103) has also demonstrated the similar behaviour as shown in Fig. 19.

Figure 17: Effects of TDR response of various bend structures

Figure 18: Surface current simulation plot (a) right angle (b) round bend

Figure 19: Near-Field emission plot (a) right angle bend (b) round bend
d) Effects of Ground Return Via Optimization

When a signal propagates through the interconnect from the source and a reference, it has to return back to the source through the same reference. While emphasis in the past has been placed significantly on the forward trace routing, the return path through the plane is often neglected. Many designers have overlooked the return ground vias in their PCB designs. However, for high-speed digital design, this aspect cannot be ignored and a return path has to be designed into the layout with as much attention as the signal path.

As it has been shown that at high frequencies, the return current follows closely to the signal path with the least loop inductance. Hence, for PCB interconnects, the path of least inductance is in fact directly next to the signal path. For transmission lines such as microstrip and strip lines where signal is driven with a common reference between them, the return path is easy to determine, as shown in Fig. 20.

![Figure 20: Two conductors microstrip interconnects over common return plane](image)

If the signal transits through a multi-layer PCB over different ground planes, the reference plane is no longer common. This gives rise to serious discontinuities problem in the return path and would lead to degradation of signal performance. The return path will go through the nearest surrounding ground via to move from ground plane 2 to ground plane 1, as shown in Fig. 21.
In this configuration, the effects of the presence of even one single ground return via can significantly affect the behaviour of the return current flow, as shown in Fig. 22.

It has been discussed in section 2.1.1 that with a four ground vias structure to accompany the signal transition as shown in Fig. 23(a), one can control the capacitance and provide optimum impedance control with excellent $S_{11}$ and $S_{21}$ performances. However, typical multilayer PCBs have easily over a thousand signal vias. The four ground via design approach will increase the number of vias significantly and causes tremendous routing constraints and often not practical. Hence, a more practical technique of using single ground via return shown in Fig. 23(b) is explored. This is a typical adopted technique. Its TDR and $S_{21}$ performances are shown in Fig. 24 and Fig. 25 respectively.
CHAPTER 2: LITERATURE REVIEW

(a)  
(b)  

Figure 23: Ground return via design (a) 4 ground vias and (b) single ground via

The study of the single via configuration [46] has shown that the optimum distance of the ground via to the signal via is around 0.35 mm to avoid signal aberration due to the impedance discontinuity when the signal transits between ground layers in the multi-layer PCB. The TDR response shown in Fig. 24 can be optimised to maintain around 55 Ω avoiding sudden impedance changes. The $S_{21}$ response in Fig. 25 shows an operating bandwidth of up to 16 GHz is achievable.

Figure 24: TDR response of one ground return via design configuration

Figure 25: $S_{21}$ response of one ground return via design configuration
2.1.3 Crosstalk of PCB Interconnects

Inter-trace electromagnetic coupling or “crosstalk” [47-49] is another major key issue in high-speed digital PCB design. As frequency of operation increases, PCB traces behave like transmission lines. When a signal propagates along the line, both the electric and magnetic fields shown in Fig. 26(a) are present in the transmission line.

![Figure 26](image)

(a) Microstrip FR-4 test structure for crosstalk simulation and measurement
(b) equivalent circuits of two parallel lines

For a pair of parallel transmission lines, their equivalent circuits are shown in Fig. 26(b). Neglecting the effects of resistance and conductance, each sub-section of transmission line of length $\Delta z$, can be described by a self-capacitance of $C\Delta z$, a self-inductance $L\Delta z$. The mutual coupling is described by a mutual capacitance $C_m\Delta z$ and mutual inductance $L_m\Delta z$, where $C$, $L$, $C_m$ and $L_m$ are the per unit length self-capacitance, self-inductance, mutual capacitance and mutual inductance, respectively.

Crosstalk refers to the coupling of the EM field between traces on the PCB, which are caused by fast changing currents and voltages during the transitions of logic states.

Crosstalk becomes significant as modern high-speed designs are densely populated due to miniaturisation in size and ever-increasing signal speeds. The unwanted couplings on adjacent traces from a signal trace are crucial in high-speed digital interface. Much work has also been carried out in the area of modelling, characterisation and analysis of crosstalk [51-55] and the techniques to minimise the effects associated with crosstalk [56-59].
To demonstrated the effect of trace to trace separation on near-end crosstalk (NEXT) and far-end crosstalk (FEXT), a full wave simulation using CST Microwave Studio on a microstrip FR-4 PCB test structure shown in Fig. 27 has been carried out. The simulated results are validated with actual time-domain measurement using the Agilent HP81134A pulse generator ($V_p = 1$V, $t_r = 0.1$ ns) and Tektronix DSO81204 high-speed real-time oscilloscope with a 12 GHz bandwidth, as shown in Fig. 28.

![Microstrip FR-4 test structure for crosstalk simulation and measurement](image)

**Figure 27:** Microstrip FR-4 test structure for crosstalk simulation and measurement

![Crosstalk validation](image)

**Figure 28:** Crosstalk validation (a) simulation results and (b) measurements
For a parallel pair of 5” microstrip structure, with a source voltage of $V_p$ of 1V and $t_r$ of 0.1 ns, the time-domain simulation of varying separation distance on the NEXT and FEXT are shown in Fig. 29(a) and Fig. 29(b), respectively. The results show that the most significant reduction in coupling occurs when the trace to trace separation is around 2W apart, where w is the trace width.

The time-domain NEXT voltage waveform is a trapezoidal pulse, where its pulse width increases with the line length. However, the FEXT pulse amplitude is not affected by the line length. On the other hand, the pulse amplitude of FEXT varies directly with the line length. In terms of pulse amplitude, FEXT is more significant than NEXT. A summary of the impacts of trace separation for both NEXT and FEXT are plotted in Fig. 30(a) and Fig. 30(b), respectively.
2.2 Device Characterization and Modelling

In the earlier section, the interconnects and their impacts on SI have been reviewed and summarised. Another important factor that affects SI performance is the device I/O impedance. While one can control the termination value at the output of the clock driver IC for impedance matching, it is still important to determine the true device output impedance under its actual operating condition in order to terminate the interconnects properly. The characteristics of the IC’s input and output impedances can be obtained from one of the following ways:

a. The model library of the design tools;
b. The vendor’s IBIS model; or
c. Through measurement.

2.2.1 Semiconductor Design Model Libraries

In semiconductor design environment, designers utilise layout tools such as Cadence Virtuoso. The design process flow allows the IC designer to choose the specific cell, pad and I/O options from the libraries that it has licensed with. This can vary with specific technologies (for examples, 0.35 μm, 0.25 μm, 0.13 μm, etc.) which also vary across the semiconductor device manufacturers, design houses and foundries.

The model from the design tool’s library (standard cell) [60-63] concerns more on the functional aspects of the gate such as the driving capability, speed and power consumption within the device with loading typically at 2-5 pF capacitance ignoring the effects of resistance, wire bonding and package lead frame. Also, external factors due to layout such as trace impedance, device loading and frequency, which affect the SI analysis, are not taken into consideration.
Most often, the main problem with these tools is that the cell libraries are only available to the IC designers within the IC design environment. These licenses are governed by strict usage control and cannot be shared outside the design environment without written license agreement and vendor approval. Hence, they are not easily available in public domain. Furthermore, the cost of the cell libraries varies from several hundred thousands dollars per library in 0.25 µm to several millions of dollars for the latest 90/65 nm technologies. To the designer, typically it may need 3-5 libraries for a specific technology, while to the foundry, it may require more and it also varies for different vendors. Hence, accessibility of the information can be extremely costly.

These models are usually not readily available to the PCB circuit, layout and SI designers. Sometimes, some device manufacturers do not clearly define its technology used in the datasheets. Even if it specifies its technology, it does not reveal its library and foundry vendor information. Worst of all, the I/O pad and cell information are not available. Hence, information pertaining to the device is only as accurate as the datasheet released by the IC manufacturer, which can be overly simplified and mainly for timing specific design purposes. Nothing or little information on SI, which is now becoming one of the key bottlenecks in high-speed product design, is available. The electrical information in typical device datasheet\* includes:

- Functional truth-table, device schematic, package and pin out;
- Absolute maximum and recommended operating conditions;
- Input and output estimated capacitance ($C_{in}$, $C_{out}$);
- DC electrical characteristics ($V_{cc}$, $V_{ih}$, $V_{il}$, $V_{oh}$, $V_{ol}$, $I_{oh}$, $I_{ol}$ etc);
- AC switching characteristics ($F_{max}$, $T_{plh}$, $T_{phi}$, $T_r$, $T_f$ etc); and
- Typical test circuit and the timing waveform.

\* Texas CDC337, IDT 49FCT805, National CGS2535
2.2.2 I/O Buffer Information Specification (IBIS) Model

IBIS (Input/Output Buffer Information Specification) is a method of providing the Input/Output device characteristics of an IC to the outside world without disclosing any proprietary circuit/process information. It can be thought of as a behavioral modelling specification suitable for digital circuit simulation that is currently used by many EDA companies. The advantages of IBIS include:

- Protection of proprietary information (process parameters, circuit design etc);
- Facilitate SI analysis before design is fabricated;
- Plenty of models available from EDA and semiconductor vendors;
- Faster simulation time compared to structural and SPICE models; and
- Common standard compatible within all industry simulation platforms.

Since its introduction by Intel in 1993 aiming at CMOS and TTL IO buffers, it has gained acceptance [67-69] with major EDA companies and several semiconductor manufacturers. An IBIS open forum has also been created to promote the application of IBIS as the simulation format and standard, which was finally adopted in December 1995 as ANSI/EIA-656 standard [65]. Some of the key information in a typical IBIS model* and a typical behavioral diagram of IBIS are given below:

- Component IBIS version, manufacturer information, package information (R_pkg, L_pkg, C_pkg);
- Component pin information (Pin no, name, model, R_pin, L_pin, C_pin);
- Model type: open sink/source, I/O drain/sink/source, I/O ECL, inverting/non-inverting, active-low/high, terminator, C_ref, R_ref, V_ref, V_meas, C_comp; and
- Model temperature, voltage range, pullup/pulldown IV, power/ground clamp IV, Rise/Fall waveform, V_in/V_inh.

* See appendix on IBIS model sample
A typical IBIS model of a device is shown in Fig. 31.

IBIS version 4.2 [66], which is the latest ratified by the IBIS open forum has become very comprehensive. This has led to further developments, such as “ICM” IBIS interconnects modelling specifications for passive interconnects “IMIC” IO interface model for IC by Japan JEITA and “ICEM” Integrated Circuit Electrical Model by IEC draft 62014-3 for EMI behavioral simulation.
**Self generated IBIS:** One can create the IBIS from measurement, data books or datasheets based on the I/V data, if available. However, in most cases, this information is too generic and may not show the actual variation that exists in the device. This may be suitable for very general circuit simulations. However, such models are not suitable for modelling in high-speed application where accuracy is critical. Generating IBIS library in-house will be extremely costly and manpower intensive. [75]

**Free IBIS model:** Many design houses and CAE vendors provide a wide range of IBIS models free of charge but users have to do their own translation or verification before using them as no one would guarantee its accuracy and validation. At many instances, even errors occur in the model syntax. For companies that have developed their own libraries, they are only available within the companies.

There are also translators and utilities (s2ibis, winibis, s2iplt, ibis_chk) available but usually not user-friendly especially for the newer version. They may still contain fixes as IBIS standard continues to evolve and all these software come from different developers or groups that may not continue to upgrade according to the latest standard.

**Problems with IBIS model:** The IBIS model has been used widely by many EDA tools at board-level circuit simulation. Unfortunately, details of the IBIS model from the semiconductor vendors are not well shared among the EDA tool developers to protect vendor proprietary design information. Although there are signs that more customers have expressed strong interests in the IBIS models, in which the semiconductor vendors have to supply these models for the devices they produced; IBIS models of many devices are still not readily available, which have been the key problems with the users [70-72].
Also, the device information given is typical value and is not guaranteed. The SPICE model may be a general one and may not reveal the details of the buffers or latest information. Hence, they are not necessary best representatives of the device. As long as information does not flow freely between the semiconductor manufacturers, designers and the EDA industries, which will expect to continue due to proprietary issues, the IBIS models will remain to be used for functional verification and lack of accuracy for SI simulation. [73-74].

2.2.3 Device Characterization through Measurement

Another possible way to extract device impedance information is through measurement. Various instruments and techniques are available in the market for impedance measurement with different degree of accuracy and frequency range. Conventionally, the measurement techniques fall under two general categories, LCR or impedance measurements.

A comparison of the different measurement techniques [76-77] is shown in Fig. 32. Their operating capabilities are briefly summarised in this section.

Figure 32: Measurement techniques and frequency range[76]
a) **Bridge Technique**

The Wheatstone bridge shown in Fig. 33 is by far the most common technique ever developed and most impedance bridges are derivative of it. It can be highly accurate (0.2 % is achievable) with a wide frequency ranges from DC to 300 MHz. The key advantage is its low cost with reasonable accuracy. However, it is only suitable for research usage and not common in industry application as it needs to be manually balanced and can be rather tedious when the measurement covers over a wide frequency range. Upon balanced condition, no current flows through the null detector (G), the unknown impedance $Z_4$ can be computed as follows:

$$Z_4 = \left( \frac{Z_1}{Z_2} \right) Z_3$$  \hspace{1cm} (2-5)

Some of the typical bridges include Wien bridge for capacitance measurement, Maxwell bridge for low-Q inductance measurement and Hay bridge for high-Q inductance measurement.

![Diagram of a Wheatstone Bridge](image)

**Figure 33:** Bridge measurement method
b) I-V Technique

For this method, a sinusoidal voltage signal from a function generator is utilised to cause a current flowing through an unknown impedance with a known resistor R, which is typically low resistance value to prevent the effect of circuit loading, as shown in Fig. 34. Since both voltage and current are needed to determine the unknown impedance, it is commonly known as I-V method. Typical I-V techniques cover from 40 to 110 MHz with a small dynamic impedance range. This technique allows in-circuit testing and hence is quite popular in device manufacturer for component characterization. The unknown impedance $Z_x$ can be determined as follow:

$$V_2 = I \times R \quad (2.6)$$

$$Z_x = \frac{V_1}{I} = \frac{V_1 \times R}{V_2} \quad (2.7)$$

![Diagram of I-V measurement method](image)

Figure 34: I-V measurement method
c) **Resonant or Roll-off Technique**

In this technique, the unknown inductor $L_x$ is placed in a circuit which is adjusted to resonate with a tuning capacitor $C$, as shown in Fig. 35. The resonant frequency can be obtained from the oscillator setting. The quality factor $Q$ can be directly measured using a voltmeter placed across the tuning capacitor. The unknown $L_x$ can be obtained from the resonant test frequency and known $C$ value.

At resonance:  
\[ \left| X_L \right| = \left| X_C \right| \equiv \omega_{osc} L_x = \frac{1}{\omega_{osc} C} \]

\[ L_x = \frac{1}{\omega_{osc}^2 C} \tag{2.8} \]

The unknown loss resistance $R_x$ can be found by:

At resonance:  
\[ Q = \frac{X_L}{R_x} = \frac{\omega_{osc} L_x}{R_x} \]

\[ R_x = \frac{\omega_{osc} L_x}{Q} \tag{2.9} \]

![Diagram of Resonant or roll-off measurement method](image)

**Figure 35**: Resonant or roll-off measurement method

This key advantage of this method is good $Q$ accuracy and therefore very suitable for high $Q$ device measurement. However, it requires manual tuning and can be tedious in measurement process. Typical measurement frequency ranges from 10 kHz to 70 MHz.
d) **Auto-Balance Bridge Technique**

This technique offers the widest impedance measurement range with typical measurement frequency from 20 to 110 MHz. The current, flowing through the unknown impedance $Z_x$, also flows through the resistor $R$ as shown in Fig. 36. The potential at point “L” is maintained at zero volts. The current through $R$ balances with the current through $Z_x$ by operation of the I-V converter amplifier. The unknown impedance $Z_x$ is calculated using voltage measurement ($V_1$) at point “H” and that across $R$ ($V_2$).

\[
I = \frac{V_2 - V_L}{R} = \frac{V_2}{R} \quad (2.10)
\]

\[
Z_x = \frac{V_1}{I} = \frac{V_1R}{V_2} \quad (2.11)
\]

![Auto balancing bridge measurement method](image)

This technique is best suited as a general purpose LCR meter for measurement below 100 kHz, which uses a simple operational amplifier for its I-V converter. At higher frequency, it requires to employ I-V converters consisting of sophisticated null detector, phase detector, integrator and vector modulator to ensure good accuracy.
e) Network Analysis Technique

Fig. 37 shows a network analysis technique offers the highest frequency coverage, but only works best when the measurement impedance range is close to 50 Ω. The reflection coefficient is obtained by measuring the ratio of an incident signal to the reflected signal. A directional coupler or a bridge is used to detect the reflected signal and a network analyzer is used to supply the incident signal and measure the reflected signal. This method is most widely used for RF and microwave component and circuit analysis with operating frequency from 300 kHz to several tens of GHz.

![Network Analysis Measurement Method and Sensitivity Comparison](image)

Reflection coefficient and the unknown impedance are determined by:

\[ \rho = \frac{V_{\text{Reflected}}}{V_{\text{Incident}}} = \frac{Z_x - Z_0}{Z_x + Z_0} \quad (2.12) \]

\[ Z_x = 50 \left( \frac{1 + \rho}{1 - \rho} \right) \quad (2.13) \]

Based on equation (2.12), reflection coefficient varies from -1 to 1. Depending on the impedance \( Z_x \), the measurement is accurate when \( Z_x \) approaches \( Z_0 \). The change in gradient of the reflection coefficient when \( Z_x \) is small and very large, is non linear causing deterioration in measurement accuracy.
f) **RF I-V Technique**

RF I-V is an enhancement of the I-V technique, offering some of the high frequency benefits of the network analysis beyond the frequency coverage of the auto-balancing bridge method while retaining some of the impedance measurement range of the I-V technique. Since RF I-V method is based on the linear relationship of voltage-current ratio to impedance given by Ohm’s law, its sensitivity is more consistent. It also offers high accuracy (~1%), wide impedance range (100 mΩ - 10 kΩ) and wide frequency dynamic range (100 kHz- 3 GHz). It is configured slightly different by using an impedance matched (50 Ω) measurement circuit and a precision coaxial test port for operation at higher frequencies. Layout is slightly different for low and high impedance measurements as shown in Fig. 38.

![Diagram of RF I-V measurement method](image)

**Figure 38:** RF I-V measurement method [76]
In summary, the various measurement techniques mentioned can be summarised as follows:

- **LCR meters:** Mainly utilise balancing bridge techniques and most of these are highly accurate for device characterization but have limited measurement frequency range up to 110 MHz. These meters are mostly used in specific spot frequency measurement and hence suitable for general purpose impedance measurement.

- **Impedance Analyzers:** Mostly utilise I-V and RF I-V techniques. They provide accurate measurement over a wide impedance range. However, they are designed mainly for LCR passive components, material and semiconductor devices measurements. They have limited measurement frequency of up to 110 MHz for I-V technique or up to 3GHz for RF I-V technique.

- **Network Analyzers:** Based on transmission/reflection techniques and offer the broadest frequency range up to 100 GHz. However, this technique only delivers exceptional accuracy when unknown impedance is near $Z_o$ (50 $\Omega$ or 75 $\Omega$) and the accuracy deteriorates for impedance either much higher or much lower than $Z_o$.

All the above mentioned commercial off the shelves (COTs) instruments for impedance measurement are available in the market, for examples, Agilent and Keithley have very comprehensive instruments for various frequency range and impedance range. Some of these are dedicated and can be rather expensive. However, most of them are not designed for in-circuit characterization other than those used in component characterization by manufacturing companies.

As most of these instruments are designed specifically for component characterization, the measurement accuracy requires critical calibration and compensation procedures [76] together with customised and often expensive test jig to ensure high accuracy. None of these instruments are intended for the actual in-circuit measurement with a device in its actual operating conditions.
3.0 REVIEW OF IMPEDANCE MEASUREMENT

Passive components such as resistors and capacitors are abundantly found in most digital circuit design. Resistors, being the most common components in digital circuits, are used for terminations, impedance matching and current flow regulation. Capacitors are also used extensively in applications such as bypassing, inter-stage coupling, filter and matching network. All integrated devices input and output are terminated by components with their impedances varied with biasing and operating frequency. In-order to match the devices to the PCB interconnects, appropriate understanding of the component impedance characteristic [90] is important to achieve the desired SI performance in high-speed digital design. This chapter reviews the high frequency behavior of the off-chip passive devices. The impedance measurement technique for components in its intended in-circuit operating condition will also be described.

3.1 High Frequency Behaviors of Passive Components

In reality, passive components are never ideal [80-81]. As components such as IC, PCB interconnects and termination resistors are used in ever-increasing operating frequency environment, their parasitic natures begin to surface. These parasitic affect the high frequency behavior of the components. Hence, it is important to take these non-ideal effects into consideration in high-speed circuit design so that proper part for impedance matching purposes can be selected.
3.1.1 High Frequency Effects on Resistor Characteristic

A resistor R is never ideal and in high frequency operation, the hidden schematic of non-ideal parasitic capacitance and inductances begin to surface, as shown in Fig. 39.

![Equivalent circuit of a non-ideal resistor](image)

Figure 39: Equivalent circuit of a non-ideal resistor [80]

The useful operating range of a resistor is defined as the highest frequency in which the impedance differs by more than that of the specified tolerance typically near its corner frequency. The characteristic of a resistor can vary significantly over the frequency range as shown in Fig. 40(a). Resistors of different values can behave differently as shown in Fig. 40(b), where the highest operating frequency of low-value resistor is limited by the lead inductance while high-value resistor is limited by the parasitic capacitance.

![Characteristics](image)

(a) (b)

Figure 40: Characteristic response (a) a 500 Ω thin-film resistor and (b) metal-film with difference values [81]
3.1.2 High Frequency Effects on Inductor Characteristic

An inductor is basically a coil formed by winding a wire on a cylindrical former to increase its magnetic flux linkage between turns of the coil. The increase in flux linkage increases the self inductances of the wires and creates an inductor. However, as frequency increases, besides the frequency dependent wire resistance, the effect of parasitic capacitance between adjacent turns begin to surface. The equivalent circuit of an inductor is shown in Fig. 41.

![Equivalen circuit of a non ideal inductor](image)

**Figure 41:** Equivalent circuit of a non ideal inductor [80,81]

The impedance of an inductor increases with frequency, as shown in Fig. 42. Beyond the resonant frequency, the influence of the parasitic capacitance becomes dominant and the impedance of the inductor decreases instead.

![Characteristic response of an inductor](image)

**Figure 42:** Characteristic response of an inductor [81]
3.1.3 High Frequency Effects on Capacitor Characteristic

Capacitors are used extensively in application such as bypassing, inter-stage coupling, filters and matching network in digital design. At high frequency, a non-ideal capacitor is in fact, a complex impedance whose equivalent circuit consists of series and parallel elements as shown in Fig. 4.3. Besides the frequency dependent wire resistance, dielectric loss due to dielectric absorption and molecular polarisation become significant at high frequencies.

![Equivalent circuit of a non ideal capacitor](image)

The impedance of a capacitor decreases with frequency. Beyond the resonant frequency, the influence of the parasitic inductance becomes dominant and the impedance increases instead, as shown in Fig. 4.4.

![Characteristic response of a capacitor](image)
3.2 Current Measurement

In general, there are three methods for current measurement. The first method inserts a current meter to the circuit under test (CUT) to obtain the current reading. This method requires one to physically break the circuit at some point, which can be cumbersome and at times impractical. The second method connects a voltage probe from an oscilloscope to a known resistor in the CUT. With the measured voltage and the known resistor value, one could calculate the current flows in the CUT. However, it requires an insertion of a known resistance in the CUT if none exist in the measurement setup, which can be inconvenient and the inserted resistor will have an impact on the CUT’s operation. The last method uses an inductive coupled clamp-on current probe so that the current of the circuit can be measured without breaking the circuit and introduced negligible loading effects to the CUT.

3.2.1 Advantages of Using Current Probe

Usage of current probes has been gaining significant attention in non-intrusive measurement. The advantages of using current probes are as follows:

- Ease of permanent or temporary installation in CUT;
- No direct electrical connection and therefore minimises loading effect to the CUT;
- Clamping type probes offer ease in test setup to measure current of the CUT under its actual operating condition; and
- Preserve fidelity of the signal without the effects caused by the conventional passive probes as the current probe couples signal magnetically rather than direct electrical connection to the measuring instrument.

3.2.2 Measuring Current Signals

A current probe is equivalent to a transformer with a small number of turns on the primary side of the conductor under test and a larger number of turns on the secondary winding that connects to the measuring instrument, usually matched at 50 Ω. When the measured current flows through the conductor in the CUT, by Faraday law, an induced current will be picked up by the instrument at the secondary coil. This is then converted into a measurable voltage. Depending on the probe sensitivity and operating bandwidth, an accurate current reading with good dynamic range and wide bandwidth can be obtained.
3.2.3 Single Probe Measurement Limitation

To obtain impedance information, one needs to know the voltage across a device as well as the current passing through it. An injecting signal from an injecting voltage probe is needed and a current probe will be used to measure the current passing through the device. Unfortunately, most single-ended voltage probes do not cover a wide frequency range due to inherent parasitic capacitances of the probes. Therefore, accurate magnitude as well as phase information at high frequency is limited by the voltage probe’s bandwidth. Although there are differential voltage probes that cover wider frequency bandwidth but the measurement setup becomes more complex and the calibration process to eliminate setup error can be tedious.

The proposed two current probes approach, though less straightforward to obtain the impedance information, has simpler test setup. Also, the convenient of the two-port measurement using the VNA, it allows the magnitude and phase information of the impedance to be extracted with relative ease. The thesis has demonstrated that through careful calibration process, the error due to the setup can be eliminated to ensure good measurement accuracy up to 1 GHz. The advantages of the use of two current probes approach for active device impedance measurement were mentioned by Roger* as follows:

- The inductive coupling of the two probes introduce negligible impedance to the device under test in its operating circuit; and
- The device under test is not interrupted during the measurement.

At frequencies below 200 MHz, where the phase variation is insignificant, scalar measurement instruments are sufficient to extract reasonably accurate impedance information, which has been reported in earlier works [82-86]. However, as frequency increases beyond 500 MHz, the phase variation due to parasitic effects of the component under test become significant and two-port S-parameters measurement using the VNA is necessary. With the two wide-band two current probes and a careful calibration process, accurate impedance extraction with both magnitude and phase information up to 1 GHz becomes possible, as demonstrated in this thesis.

---

3.3 In-Circuit Measurement using Two Current Probes

The method of using two current probes in impedance measurement has long been utilised since the mid 60s and much work and research has been done by various researchers and industrial engineers since. Some of the earlier works include that by Brooks\(^*\) [82] in 1965 for the measurement of power-line impedances in frequencies ranging from 20 kHz to 30MHz. This was later improved with calibration techniques for current probe losses by Southwick [83] in 1971 and RF impedance of power lines and LISN in conducted interference work by Nicholson and Malack [84] in 1973. Much research was done in the application of current probe measurement for power device in frequency less than 100MHz. [85-86]. Later improved techniques for power line impedance up to 500 MHz was reported [87-89]. However the results from the reference paper [88] extracted here clearly shows its accuracy deteriorates when the frequency goes beyond 500MHz significantly.

There is an increasing need for extending the frequency range up to 1GHz or beyond for high frequency in-circuit characterisation due to rapid increase in operating frequency of high-speed circuits. In this thesis, by introducing a careful and dedicated calibration process, the error due to measurement setup above 500 MHz can be eliminated. It is demonstrated that the two current probes method can be extended up to 1 GHz to characterise both the non-linear passive component as well as the active device output impedance with very good accuracy.

* This was the earliest known literature by the author. There may be other research works or published literatures in this area that the author is unaware.
3.3.1 High Frequency Current Probe

The CT6 current probe [78, 79] from Tektronix is a current probe designed and optimised for very high frequency operation. It was chosen for our research work as it has wide bandwidth, low inductance and very small form factor. The key specifications of the CT6 current probe are:

- Wide bandwidth up to 1.5 GHz;
- Low leakage inductance of 1.5 nH;
- High sensitivity of 5 mV/mA;
- Ability to detect short rise time of 200 ps;
- Accuracy of +/- 3%;
- Maximum peak pulse current of 6A and maximum continuous current (rms) of 120mA without saturation;
- Low insertion impedance (1.1 Ω @ 10 MHz, 1.3 Ω @ 100 MHz & 12 Ω @ 1 GHz);
- and
- Accept un-insulated wire size up to 20 gauge

3.3.2 Injecting Current Signals

In the two current probes technique proposed, a second current probe will be configured for signal injection. When used for injecting AC current into a conductor in the circuit under test (CUT), the current probe acts as the primary winding connecting to the signal injection source. The conductor in the CUT acts as the secondary winding of the transformer. The current probe converts the voltage signal on the primary side to a current signal in the current carrying conductor in the CUT.
3.3.3 Measurement Setup for Optimum High Frequency Performance

Several important issues have to be taken into consideration when using the current probe to ensure measurement accuracy. These issues are briefly summarised here:

- **Current probe transfer impedance**

  Every current probe is characterised individually with a transfer impedance. The frequency response of the transfer impedance has to be observed carefully in order to utilise the probe within its suitable bandwidth of operation for best accuracy. As for CT6, though its specification covers a typical bandwidth of 250 kHz to 2 GHz as shown from the transfer impedance plot in Fig. 45, it is clear that at both the lower and upper end of the frequency, the response deteriorates. Hence, to achieve best accuracy, the desired frequency range of operation should be limited from 2 MHz to 1 GHz.

![CT6 Typical Frequency Response](image)

Figure 45 : CT6 probe frequency response [78]
CHAPTER 3: REVIEW OF IMPEDANCE MEASUREMENT

- **Wire size and length**
  The wire gauge and length of the wire used to route the test current through the probe have a direct effect on the amount of stray capacitance and inductance it introduce. The longer the wire, the higher the stray inductance and it adds to the circuit impedance at high frequency. It is recommended that a length not longer than 1 cm be used. The larger the gauge size of the wire, the more stray capacitance exists between the wire and the current probe. The probe, though designed to measure magnetic field, is also sensitive to stray electric field pick up by the stray capacitance. This affects the CUT at high frequency and adds aberrations to high frequency signals. It is best to use a wire with the smallest possible diameter and the recommended wire size should be larger than 27 gauge.

- **Positioning of probe**
  Each probe also has stray capacitance associated with the case that surrounds the head of the current probe when there is a wire with a relatively large diameter in the probe (approximately 20 to 25 gauges). When measuring high-frequency signals with a wire of larger diameter, it is generally best to position the probe head perpendicular to the circuit board under test as shown in Fig. 46.

![Figure 46: CT6 positioning for HF application [79]](image)
3.3.4 Theoretical Background of Two-Probe Measurement

Unlike the impedance measurement using the conventional voltage probe, with current probe, the measurement using two current probes requires several steps. The concept of measuring unknown impedance $Z_x$ seen at $x-x'$ using the two-probe approach can be illustrated by the test setup shown in Fig. 47(a) [85-86]. It consists of an injecting current probe, a receiving current probe and a vector network analyzer (VNA). The two probes are inductively coupled to the circuit without direct connection to $Z_x$, hence minimizing loading to CUT.

![Diagram](image)

**Figure 47:** (a) Basic test setup; (b) equivalent circuit of two probes measurement
The equivalent circuit of the two probes setup is shown in Fig. 48(b). $V_1$ is the output signal source voltage of port 1 of the network analyzer connected to the injecting probe, and $V_2$ is the resultant signal voltage measured at port 2 of the network analyzer with the receiving probe. Impedances of the VNA ports are usually 50 Ω while $Z_1$ and $Z_2$ are the matching impedances to the injection and receiving probes seen by ports 1 and 2, respectively. $L_1$ and $L_2$ are the primary self-inductances of the injecting and receiving probes respectively, and $L$ is the loop inductance of the circuit under test. $M_1$ is the mutual inductance of the injecting probe and the CUT loop, and $M_2$ is the mutual inductance between the receiving probe and the CUT loop. The induced voltage at the unknown impedance $Z_x$ is $V$ and the induced current through $Z_x$ is $I$.

(i) Equivalent Circuit of Injection Probe:
Without the receiving current probe, the injecting probe induces a signal current $I_i$ in the CUT and causes a signal voltage $V_i$ across $Z_x$ as shown in Fig. 48.

\[
V_1 = (50 + Z_1 + j\omega L_1)I_i - j\omega M_1 I_i
\] (3.1)

Figure 48 : Equivalent circuit of the injection probe

At the primary side of the injecting probe:
At the secondary side of the injection probe:

\[ I_i (j\omega L + r + Z_x) - j\omega M_1 I_i = 0 \]  \hspace{1cm} (3.2)

From (3.1):

\[ I_1 = \frac{V_i + j\omega M_1 I_i}{(50 + Z_1 + j\omega L_1)} \]  \hspace{1cm} (3.3)

Sub (3.3) into (3.2) and eliminating \( I_1 \),

\[ I_i (j\omega L + r + Z_x) - j\omega M_1 \left( \frac{V_i + j\omega M_1 I_i}{50 + Z_1 + j\omega L_1} \right) = 0 \]

\[ I_i (j\omega L + r + Z_x) - \frac{j\omega M_1 V_i}{50 + Z_1 + j\omega L_1} + \frac{(\omega M_1)^2 I_i}{50 + Z_1 + j\omega L_1} = 0 \]

\[ I_i (j\omega L + r + Z_x) - V_{M1} + I_i Z_{M1} = 0 \]

\[ V_{M1} = I_i (j\omega L + r + Z_{M1} + Z_x) \]  \hspace{1cm} (3.4)

where

\[ Z_{M1} = \frac{(\omega M_1)^2}{50 + Z_1 + j\omega L_1} \]  \hspace{1cm} (3.5)

\[ V_{M1} = \frac{j\omega M_1 V_i}{50 + Z_1 + j\omega L_1} \]  \hspace{1cm} (3.6)

From (3.4), the injection probe in Fig. 48 is reflected in the CUT loop and represented by Fig. 49.

---

**Figure 49:** Reflected equivalent circuit of injection probe in CUT loop
(ii) Full Equivalent Circuit in the Coupled Circuit Loop:

With the addition of the receiving current probe, it introduces another impedance reflected in the CUT. The final equivalent circuit of Fig. 47(b) is given in Fig. 50, where $Z_{M2}$ is the reflected impedance in the CUT due to the receiving probe.

\begin{figure}[h]
\centering
\includegraphics[width=0.9\textwidth]{figure50.png}
\caption{Final reflected equivalent circuit of the two probes measurement setup}
\end{figure}

From Fig. 50, the resultant induced current in the CUT loop due to the injecting signal is given by:

\[ I = \frac{V_{M1}}{Z_{M1} + Z_{M2} + j\omega L + r + Z_x} \quad (3.7) \]

$Z_{M1}$ and $Z_{M2}$ are the impedances due to the two probes, while $r$ and $j\omega L$ are the resistance and inductive reactance of the connecting conductors to $Z_x$. By defining $Z_{\text{setup}}$ as the impedance due to the measurement setup,

Then $Z_{\text{setup}} = Z_{M1} + Z_{M2} + j\omega L + r$ and equation (3.7) can be rewritten as:

\[ I = \frac{V_{M1}}{Z_{\text{setup}} + Z_x} \quad (3.8) \]

From (3.8), the unknown $Z_x$ can be obtained by:

\[ Z_x = \frac{V_{M1}}{I} - Z_{\text{setup}} \quad (3.9) \]
The induced current measured by the receiving probe can be determined by:

\[ I = \frac{V_2}{Z_{r2}} \]  

(3.10)

where \( Z_{r2} \) is the calibrated transfer impedance of the receiving current probe, which is defined as the ratio of the voltage measured by the probe and the current flowing through the probe. The calibrated \( Z_{r2} \) versus frequency can be found in the current probe data sheet [78]. Substituting (3.6) and (3.10) into (3.9):

\[ Z_x = \left( \frac{j \omega M_1 V_1}{50 + Z_1 + j \omega L_1} \right) \frac{Z_{r2}}{V_2} - Z_{\text{setup}} \]  

(3.11)

Let \( k = \frac{j \omega M_1 Z_{r2}}{50 + Z_1 + j \omega L_1} \), then (3.11) becomes:

\[ Z_x = \frac{k V_1}{V_2} - Z_{\text{setup}} \]  

(3.12)

(iii) Determination of the coefficient \( k \) and \( Z_{\text{setup}} \):

From (3.12), \( Z_x \) can be determined if \( k, V_1/V_2 \) and \( Z_{\text{setup}} \) are known. \( V_1 \) and \( V_2 \) relates to the signal voltages of the injecting and receiving probes and can be obtained by the VNA, \( V_1 \) and \( V_2 \) are related by:

\[ \frac{V_2}{V_1} = \left( \frac{S_{21}}{1 + S_{11}} \right) \]  

(3.13)
where $S_{11}$ and $S_{21}$ are the reflection and insertion losses respectively, obtained from the VNA. The magnitude and phase for (3.13) can be obtained as follows [112]:

**Magnitude:**

$$\left| \frac{V_2}{V_1} \right| = \frac{|S_{21}|}{1 + |S_{11}|} = \frac{|S_{21}|}{\sqrt{(1 + |S_{11}| \cos \angle S_{11})^2 + (|S_{11}| \sin \angle S_{11})^2}}$$

(3.14)

**Phase:**

$$\angle \frac{V_2}{V_1} = \angle \frac{S_{21}}{1 + S_{11}} = \angle S_{21} - \tan^{-1}\left( \frac{|S_{11}| \sin \angle S_{11}}{1 + |S_{11}| \cos \angle S_{11}} \right)$$

(3.15)

From the expression of $k$, we know that it depends on the characteristic of the probes and the coupling between probes and the CUT. Hence, we can perform a pre-measurement calibration process to determine $k$ and $Z_{\text{setup}}$ under two known conditions. Firstly by replacing $Z_x$ in (3.12) with a short circuit ($Z_x = 0$ Ω):

$$0 = k \left( \frac{V_1}{V_2} \right)_{Z_x=0} - Z_{\text{Setup}}$$

$$Z_{\text{Setup}} = k \left( \frac{V_1}{V_2} \right)_{Z_x=0}$$

$$k = Z_{\text{Setup}} \left( \frac{V_2}{V_1} \right)_{Z_x=0}$$

(3.16)

Next by replacing $Z_x$ in (3.12) with a known precision standard resistor $R_{\text{std}}$, we have:

$$R_{\text{std}} = k \left( \frac{V_1}{V_2} \right)_{Z_x=R_{\text{std}}} - Z_{\text{Setup}}$$

(3.17)
Substituting (3.16) in (3.17) and eliminating $k$, $Z_{\text{setup}}$ can be determined by:

$$R_{\text{std}} = Z_{\text{Setup}} \left[ \frac{V_2}{V_1} \right]_{Z_X = 0} \left[ \frac{V_1}{V_2} \right]_{Z_X = R_{\text{std}}} - Z_{\text{Setup}}$$

$$R_{\text{std}} = Z_{\text{Setup}} \left[ \left( \frac{V_2}{V_1} \right)_{Z_X = 0} \left( \frac{V_1}{V_2} \right)_{Z_X = R_{\text{std}}} - 1 \right]$$

$$Z_{\text{Setup}} = \frac{R_{\text{std}}}{\left[ \left( \frac{V_2}{V_1} \right)_{Z_X = 0} \left( \frac{V_1}{V_2} \right)_{Z_X = R_{\text{std}}} - 1 \right]}$$

(3.18)

Substituting (3.18) into (3.16), $k$ can be obtained as follows:

$$k = \left[ \left( \frac{V_2}{V_1} \right)_{Z_X = 0} \left( \frac{V_1}{V_2} \right)_{Z_X = R_{\text{std}}} - 1 \right]$$

(3.19)

Hence, by measuring $\left( \frac{V_2}{V_1} \right)_{Z_X = 0}$ and $\left( \frac{V_1}{V_2} \right)_{Z_X = R_{\text{std}}}$, $Z_{\text{setup}}$ and $k$ can be determined from (3.18) and (3.19), respectively. Once $Z_{\text{setup}}$ and $k$ are found, the two-probe setup is ready to measure any unknown impedance $Z_x$ through (3.12). This calibration process allows the impedance due to the test setup to be eliminated or minimised for good measurement accuracy. However, it is important to note that the choice of known precision standard resistor $R_{\text{std}}$ has to be carefully chosen such that its impedance remains constant and frequency independent up to the maximum frequency of interest so as to ensure a proper calibration process. The chosen standard resistor has to be measured with an impedance analyser to ensure that its impedance remains flat over the frequency range of 30MHz to 1GHz.
Chapter 4

4.0 VALIDATION OF TWO-PROBE MEASUREMENT METHOD

In order to validate the proposed measurement method using the two current probes approach, the impedance of a few passive components under direct current (DC) biasing condition will be used as test cases for in-circuit measurement. It will be shown later that with a pre-measurement calibration process described in Chapter 3, the proposed method has the ability to eliminate the error due to the measurement setup so as to achieve good measurement accuracy.

Using several resistors and inductors as devices under test, impedance characterization of each passive component up to 1 GHz with good accuracy has been demonstrated [117]. The two-probe measurement approach also provides insight to the impedance behavior of a critical circuit component under its intended in-circuit condition so that proper choice of component can be made for a specific biasing condition to achieve optimal circuit performance. It also allows a designer to perform component sensitivity analysis due to part changes from existing design and to investigate the impact of impedance deviation from the original design to avoid unwanted variation or drift in circuit behavior that causes failure in the functional specifications of the circuit.
4.1 In-Circuit Characterization of Passive Components

With the trend of increasing operating frequency of the electronic circuit, the impedance characteristic of a critical component up to GHz range becomes important for the circuit designers [90-92]. For example, if the applied biasing current is too high, the ferrite-core of the inductor may become saturated and its impedance can be very different from that when measured off-circuit without applied biasing. The core saturation causes a reduction in inductance of the inductor, which in turn, leads to lower inductive reactance\(^1,2\). The proposed two current probes method has the ability to detect such behaviour of a ferrite core inductor under in-circuit operating condition and the details are discussed in Section 4.5. Hence, impedance characterization of a critical circuit component with possible non-linear behaviour over a wide frequency range under its intended DC biasing condition serves as a useful assessment of the component for optimal circuit performance.

Conventional impedance measurement of a passive component requires direct electrical contact to the component, such as impedance analyzer, LCR meter and vector network analyzer (VNA) [76-77, 89]. However, such instruments are usually designed for off-circuit impedance measurement. Currently, most component characterization techniques still require direct electrical contact [93-95]. To minimise the measurement error contributed by the electrical contact to the component under test, dedicated and advanced micro probing is necessary and therefore is very costly [96-97].

The purpose of this section is to validate the proposed non-contact two-probe inductive coupling measurement technique to characterise a passive component under specific DC biasing in-circuit condition. The proposed method requires no direct electrical contact to the CUT and therefore its influence to the circuit operation is negligible. Most importantly, with a proper pre-measurement calibration of the test jig, the error contributed by the measurement setup can be eliminated to ensure good impedance measurement accuracy.

---

4.2 Measurement Setup for Validation

The measurement setup consist of an in-house designed test jig that is capable of measuring passive components over a wide range of impedance values accurately from 1 MHz to 1GHz, using the proposed two current probes technique under in-circuit operating condition.

The schematic of the measurement setup for a device-under-test (DUT) is shown in Fig. 51(a). A DC power supply and a load resistor R provide the necessary DC biasing current for the DUT. C₁ and C₂ (both 0.22 μF SMD tantalum) serve as low-impedance bypass capacitors for the injected AC signal. To facilitate the measurement without direct electrical contact, two identical inductive coupling probes (Model: Tektronix CT-6, bandwidth 250 kHz to 2 GHz), one as injecting probe and another as receiving probe, are coupled to the circuit without direct electrical contact. Port 1 of a VNA (Model: R&S ZVB8, bandwidth 150 kHz to 8.5 GHz) injects an AC signal into the circuit loop through the injecting probe and port 2 of the VNA measures the resulting coupled signal in the circuit loop through the receiving probe.

A test jig using a FR-4 printed circuit board (PCB) is fabricated, as shown in Fig. 51(b). The lower side of the PCB is a complete metal layer serving as a low-impedance signal return path. The DC power supply (Model: Caltron PR 3504D) is connected to a SMA connector and provides the DC biasing current to the DUT through a microstrip trace of length 2 cm, which is much shorter than the wavelength of the highest frequency of measurement (1 GHz). Two pairs of very short jumpers (less than 5 mm) are designed to fix the positions of the two probes to ensure measurement repeatability.
The purpose of the coupling capacitors ($C_1$ and $C_2$) is to provide the low-impedance path for the injected AC signal without affecting the DC biasing current. The value of the capacitor is chosen at 0.22 μF such that its impedance is sufficiently low to the lowest injected signal frequency.

The purpose of the load resistor is to provide a path for the DC biasing current for the DUT. Its value should be sufficiently large enough compared to the capacitive reactance of the capacitor as it is placed in parallel to $C_2$. It is to ensure the resistor $R$ is AC shorted by $C_2$. The value is chosen to be 100 Ω. The DC biasing current can be adjusted through varying the DC output voltage of the power supply.
4.3 Equivalent Circuit of the Test Setup

The equivalent circuit of the test setup shown in Fig. 51(a) can be illustrated in Fig. 52. $Z_{DUT}$ is the impedance of the DUT, $Z_{PS}/Z_{C1}$ is the parallel impedance of the power supply and bypass capacitor $C_1$, and $Z_{R}/Z_{C2}$ is the parallel impedance of the resistor $R$ and bypass capacitor $C_2$. $V_1$ is the output signal source voltage of port 1 of VNA, which is connected to the injecting probe; and $V_2$ is the resultant signal voltage measured at port 2 of VNA through the receiving probe. $Z_1$ and $Z_2$ are the matching impedances to the injecting and receiving probes seen by ports 1 and 2 respectively. $L_1$ and $L_2$ are the self-inductances of the injecting and receiving probes respectively. $L$ and $r$ are the self-inductance and resistance of the connecting copper traces that form the coupled circuit loop respectively. $M_1$ is the mutual inductance between the injecting probe and the coupled circuit loop and $M_2$ is the mutual inductance between the receiving probe and the coupled circuit loop.

![Figure 52: Equivalent circuit for the in-circuit measurement setup](image-url)
Applying KVL for the circuit of port 1 of VNA and the injecting probe,

\[ V_1 = (50 + Z_1 + j\omega L_1)I_1 - j\omega M_1 I_x \quad (4.1) \]

Applying KVL for the circuit of port 2 of VNA and the receiving probe,

\[ (50 + Z_2 + j\omega L_2)I_2 + j\omega M_2 I_x = 0 \quad (4.2) \]

Finally, applying KVL for the coupled circuit loop,

\[ I_x (r + j\omega L + Z_R \parallel Z_{C2} + Z_{PS} \parallel Z_{C1} + Z_{DUT}) - j\omega M_1 I_1 + j\omega M_2 I_2 = 0 \quad (4.3) \]

Substituting (4.1) and (4.2) into (4.3) and eliminating I_1 and I_2 leading to:

\[ I_x (r + j\omega L + Z_R \parallel Z_{C2} + Z_{PS} \parallel Z_{C1} + Z_{DUT}) - V_{M1} + I_x (Z_{M1} + Z_{M2}) = 0 \quad (4.4) \]

where

\[ V_{M1} = \frac{j\omega M_1 V_1}{50 + Z_1 + j\omega L_1}, \quad Z_{M1} = \frac{(\omega M_1)^2}{50 + Z_1 + j\omega L_1} \quad \text{and} \quad Z_{M2} = \frac{(\omega M_2)^2}{50 + Z_2 + j\omega L_2} \]

\( V_{M1} \) is the induced signal source into the circuit loop from the injecting probe, and \( Z_{M1} \) and \( Z_{M2} \) are the reflected impedances from the injecting and receiving probes into the circuit loop respectively. With these reflected signal source and impedances into the circuit loop, the equivalent circuit in Fig. 52 can be reduced to that in Fig. 53, and the resultant induced current into the circuit loop is given by:

\[ I_x = \frac{V_{M1}}{Z_{M1} + Z_{M2} + (r + j\omega L) \parallel Z_R \parallel Z_{C2} + Z_{PS} \parallel Z_{C1} + Z_{DUT}} \quad (4.5) \]
Chapter 4: Validation of Two-Probe Measurement Method

Figure 53: Simplified equivalent circuit for the measurement setup

Similar to the derivation from Chapter 3, the unknown impedance $Z_{DUT}$ can be obtained with equation (4.6):

$$Z_{DUT} = \frac{kV_1}{V_2} - Z_{\text{setup}}$$  \hspace{1cm} (4.6)

where

$$Z_{\text{setup}} = Z_{M1} + Z_{M2} + (r + j\omega L) + Z_R // Z_{C2} + Z_{PS} // Z_{C1}$$

The ratio of $V_2$ and $V_1$ can be easily measured with the VNA. To obtain the two unknown $k$ and $Z_{\text{setup}}$, we have to perform a pre-measurement calibration process before the actual measurement of $Z_{DUT}$. By replacing $Z_{DUT}$ with a short circuit ($Z_{DUT} = 0 \ \Omega$) and a known precision standard resistor $R_{\text{std}}$ ($Z_{DUT} = R_{\text{std}} \ \Omega$), $k$ and $Z_{\text{setup}}$ can be obtained using the procedure describe in Chapter 3. A precision standard 51 $\Omega$ SMT resistor is chosen as $R_{\text{std}}$.

Once $k$ and $Z_{\text{setup}}$ are found, the measurement setup is ready to measure $Z_{DUT}$ using (4.6). The magnitudes of $Z_{\text{setup}}$ and $k$ of the test jig versus frequency up to 1 GHz are determined and plotted in Fig. 54 and Fig. 55 respectively.
Fig. 54 shows that $Z_{\text{setup}}$ is very low and resistive in nature until about 100 MHz, where the inductive effect (equivalent series inductances of $C_1$ and $C_2$ and the inductance of the coupled circuit loop) of the measurement setup begins to kick in. Based on the impedance magnitude versus frequency above 100 MHz, it is found that the total equivalent inductance due to the setup is about 5 nH. With this known $Z_{\text{setup}}$, the effect due to the measurement setup can be eliminated later while determining $Z_{\text{OUT}}$.

![Magnitude of $Z_{\text{setup}}$ versus frequency](image)

**Figure 54:** Magnitude of $Z_{\text{setup}}$ versus frequency

Fig. 55 shows that $k$ remains nearly constant at 1 up to 200 MHz and increases with frequency above 200 MHz. From Chapter 3, it is known that $k = j\omega M_1 Z_{T2}/(50 + Z_1 + j\omega L_1)$, i.e. $k$ is the ratio of $j\omega M_1 Z_{T2}$ and the impedance of the primary circuit of the injecting probe. The transfer impedance of the receiving probe, $Z_{T2} = 5 \Omega$ and stays constant from 500 kHz to 1 GHz, as given in the CT6 probe datasheet. Hence, $j\omega M_1 Z_{T2}$ is directly proportional to $\omega$. The injecting current probe is basically a transformer with multi-turn primary and single turn secondary. The relatively high inductance of the primary coil of the probe causes the impedance in the primary circuit to be dominated by $j\omega L_1$. As both the terms $j\omega M_1 Z_{T2}$ and $j\omega L_1$ are proportional
to $\omega$, $k$ becomes a frequency-independent constant. However as frequency increases above 200MHz, the effect of the parasitic capacitance of the primary coil of the injecting probe begins to show its effect and its impedance in the primary circuit will be dominated by the 50 $\Omega$. Hence $k$ will be the ratio of $j\omega M_1 Z_{T2}$ and 50 $\Omega$, which becomes frequency dependent and increases with frequency.

![Graph showing the magnitude of $k$ versus frequency](image)

Figure 55: Magnitude of $k$ versus frequency
4.4 Resistor Measurement Results

For validation purposes, several selected known precision resistors are treated as unknown DUT and measured using the proposed measurement method. The following three sets of measurements are conducted for validation purposes. These include:

- Nominal impedance measurement at 1MHz;
- Full frequency range impedance response; and
- Impedance response with varying DC biasing.

4.4.1 Nominal Impedance Measurement

The impedance of each of these resistors is measured at 1 MHz using the proposed method without applied DC biasing. The same resistors are also measured directly with a HP 4192A LF Impedance Analyzer (100 kHz to 13 MHz), which is capable of measuring a wide range of resistance between 1 Ω and 1 MΩ with a resolution of 0.01% of the full-scale of the selected range [98]. The comparison of measured impedance using both methods is given in Table 1. The deviation is found to be less than 3.5 % for a wide range of resistors from 30 Ω to 2 kΩ.

<table>
<thead>
<tr>
<th>Stated Value of Resistor (Ω)</th>
<th>Measured with HP4192A (Ω)</th>
<th>Measured with Proposed Method (Ω)</th>
<th>Deviation</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 ± 1%</td>
<td>30.35</td>
<td>30.31</td>
<td>-0.1%</td>
</tr>
<tr>
<td>51 ± 1%</td>
<td>50.89</td>
<td>50.24</td>
<td>-0.7%</td>
</tr>
<tr>
<td>100 ± 1%</td>
<td>100.5</td>
<td>96.85</td>
<td>-3.4%</td>
</tr>
<tr>
<td>220 ± 1%</td>
<td>222.0</td>
<td>227.15</td>
<td>+2.3%</td>
</tr>
<tr>
<td>510 ± 1%</td>
<td>512.0</td>
<td>504.24</td>
<td>-1.5%</td>
</tr>
<tr>
<td>1K ± 1%</td>
<td>1002.0</td>
<td>1030.3</td>
<td>+2.8%</td>
</tr>
<tr>
<td>2K ± 1%</td>
<td>2007.0</td>
<td>1954.8</td>
<td>-2.5%</td>
</tr>
</tbody>
</table>
4.4.2 Full Frequency Range Impedance Response

For the complete impedance characterization up to 1 GHz, the impedance versus frequency using the proposed method for two precision resistors (30 Ω and 220 Ω) without DC biasing is measured. Measurement setup is shown in Fig. 56(a). For comparison purposes, the two resistors are measured again using a HP4396B impedance analyzer (bandwidth 1.8 GHz) together with a HP 43961A RF Impedance Test Kit and the HP16194A Component Test Fixture. The integrated instrumentation setup is shown in Fig. 56(b).

![Measurement setup](image1)

(a)  

![Instrumentation setup](image2)

(b)

Figure 56: Impedance profile characterisation validation (a) propose two probe test setup and (b) instrumentation setup using Impedance analyzer

Fig. 57(a) and Fig. 57(b) show the comparison of the two methods which clearly correlates well to the high frequency behaviour of a typical non-ideal resistor. Good agreement is observed between the two methods. The inductive behaviour of the 30 Ω resistor is expected, which is inherent for low-resistance resistor. For larger resistor, the parasitic capacitance will cause the dip in the impedance at higher frequency, which is more significant in larger value resistance.
Figure 57: Comparison of impedance versus frequency (a) 30 \( \Omega \) and (b) 220 \( \Omega \) resistor
4.4.3 Impact of DC Biasing on the Impedance Response

To demonstrate the useful feature of the proposed two-probe approach, the resistor is placed under a specific DC biasing condition and measurement taken to study the effects of the DC biasing on the impedance frequency response. For subsequent analyses, only the magnitudes of the impedance of the resistors will be shown, as the phases remain relatively unchanged. The 220 Ω resistor is chosen as the component for demonstration purposes. Its impedance under no biasing, 5 mA and 15 mA biasing are measured up to 1 GHz and shown in Fig. 58. As expected, the DC biasing current has practically no impact on the impedance response of the resistor.

![220Ω Resistor](image)

**Figure 58**: Impedance versus frequency of a 220 Ω resistor under various biasing conditions (0 mA, 5 mA and 15 mA)
4.5 **Inductor Measurement Results**

For further validation, a set of inductors was measured using the same two probes approach. Using the same in-house developed test jig, three sets of measurements are conducted on each passive inductor as follows:

- Nominal inductance measurement;
- Full frequency range impedance response; and
- Impedance response with varying DC biasing.

4.5.1 **Nominal Inductance Measurement**

A set of axial inductors (ASJ 1315 series, moulded, wire wound, ferrite core) were measured using the two probes approach. The inductance can be obtained from the measured impedance well below the self-resonant frequency. Hence, for comparison purposes, the inductance of each inductor is calculated based on the measured impedance at 2 MHz. The calculated inductance will be compared to that obtained using the HP 4192A LF Impedance Analyzer (100 kHz to 13 MHz). Table 2 shows the comparison and the deviation is within 10%. The current probe (CT6) has lower roll-off frequency response around 2 MHz (see Fig. 45). For larger value inductors, the self-resonant frequency is lower and closer to the 2 MHz measurement limits of the CT6 probe, hence higher deviation is expected. However for smaller inductance (< 47 uH) with higher self-resonant frequency which is further away from 2 MHz,, the measured inductance is more stable and the deviation is around 5%.

<table>
<thead>
<tr>
<th>s/n</th>
<th>Ref</th>
<th>Measured L Using HP 4192A (µH)</th>
<th>Measured L using two probes setup (µH)</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>L250u</td>
<td>275.3</td>
<td>303.4</td>
<td>10.21%</td>
</tr>
<tr>
<td>2</td>
<td>L150u</td>
<td>155.5</td>
<td>149.6</td>
<td>3.79%</td>
</tr>
<tr>
<td>3</td>
<td>L100u</td>
<td>97.1</td>
<td>104.7</td>
<td>7.80%</td>
</tr>
<tr>
<td>4</td>
<td>L47u</td>
<td>48.0</td>
<td>50.7</td>
<td>5.62%</td>
</tr>
<tr>
<td>5</td>
<td>L22u</td>
<td>23.8</td>
<td>22.6</td>
<td>5.04%</td>
</tr>
<tr>
<td>6</td>
<td>L2.2u</td>
<td>2.46</td>
<td>2.32</td>
<td>5.60%</td>
</tr>
</tbody>
</table>
4.5.2 Full Frequency Range Impedance Response

For validation purposes, the proposed method is used to measure a 2.2 μH inductor (ASJ 4425-10K, moulded, wire wound, ferrite core, and 10% tolerance) without DC biasing. This inductor is chosen as it has a higher self-resonant frequency so that its impedance behaviour across a wide frequency range can be observed. The inductor is measured with the HP4396B impedance analyzer (bandwidth 1.8 GHz) together with a HP 43961A RF Impedance Test Kit and the HP 16194A Component Test Fixture. The comparison using both methods is shown in Fig. 59, with close agreement between the two methods. Both measurement methods show clearly, a self resonant frequency of around 200 MHz.

![2.2uH Inductor](image)

Figure 59: Comparison of impedance versus frequency of a 2.2 μH inductor
4.5.3 Impact of DC Biasing on the Impedance Response of the Inductor

In general, ferrite core inductor’s impedance characteristic can be affected by the DC biasing when the biasing current becomes too high. The proposed method is employed to study the impedance behaviour of an inductor with varying DC biasing. Two inductors, 250 μH and 47 μH (ASJ 1315 series, moulded, wire wound, ferrite core and 5%) are selected for validation purposes. For subsequent comparisons, only the impedance magnitude will be shown. The measured impedance for 250 μH and 47 μH inductors under three different biasing conditions (0 mA, 5 mA and 15 mA) are presented in Fig. 60(a) and Fig. 60(b), respectively. The measured results show clearly that the impedance behaviour does not change much for no biasing and 5 mA biasing. However, when the DC biasing current increases to 15 mA, both inductors suffered significant drop in impedance, which is a clear indication of core saturation of the inductors. Hence, the ability to detect changes in the impedance characteristic of a component under varied biasing condition using the two-probe method has been demonstrated.

![Impedance Behavior Graph](image.png)
In conclusion, the proposed in-circuit measurement method has demonstrated its ability to measure the impedance of any passive component under its in-circuit operating condition with different biasing conditions over a wide frequency range. As expected, the biasing current has little influence in the impedance behaviour of a resistor, which is basically a linear device. However, for a passive component that exhibit non-linear behaviour, for example, a ferrite-core inductor, the impedance can vary under different biasing conditions. The measured impedance results in Section 4.5.3 has demonstrated that the impedance of the ferrite-core inductor changes significantly with differential biasing currents. This allows a designer to perform component sensitivity analysis due to a new part changes for an existing design. Any significant impedance deviation from the original component part enables the designer to ensure the correct selection of component in the circuit, so as to avoid unwanted deviation or drift in functional specifications. For example, the impact of the change of an inductor part on a filter’s response under a specific DC biasing condition.
5.0 MEASUREMENT OF ACTIVE DEVICE IMPEDANCE FOR SI ANALYSIS

The concept of transmission line, reflection and techniques for impedance matching are discussed. With the help of lattice diagram, we explain why signal distortion in a form of ringing is observed and why do we need to perform termination for impedance matching. The two-probe approach is extended to the characterisation of the output impedance of active clock drivers to understand its impact on the selection of the output series terminations for optimal SI performance. The two-probe approach will be employed to characterise the output impedance of a clock driver so that appropriate series termination can be selected systematically [118].

5.1 Transmission Line, Reflections and Impedance Matching

As mentioned in Chapter 1, the importance of interconnects termination designs in high-speed digital design is crucial for SI performance. With integrated circuits (ICs) operating at much faster edge rates (<1ns), PCB trace behave likes transmission lines and proper terminations to ensure good impedance matching become indispensable for functional reliability in high-speed digital systems. Excessive and prolong overshoot can damage devices, and together with undershoot, they cause eye closure in the eye diagram, which can lead to intermittent data error or false triggering.

5.1.1 Transmission line

In transmission line behavior, reflections at impedance discontinuity give rise to signal degradation often looks like ringing. In today tight noise margin, if the ringing is severe enough, when the undershoot at high level goes below the threshold or when the overshoot at low level bounce above the threshold, this will cause intermittent and false triggering which is highly undesirable.
5.1.2 Transient Reflections

In transmission line theory, two important concepts when a signal travels down a transmission line, part of the signal is transmitted and when impedance mismatch occurs, part of the signal is reflected. This transmission and reflection is function of load and source impedance. Referring to Fig. 62, the source impedance of a signal source is $R_s$, the load impedance of a receiver is $R_L$, and the transmission line of characteristic impedance of $Z_0$ connects the source and the receiver.

Figure 61: A 10MHz clock signal measured at a mismatch transmission trace.

Hence to prevent reflections and signal distortion due to impedance mismatch or discontinuity, its important to control the PCB board trace impedance often know as impedance control board which is fast becoming a requirement instead of a mere good to have, due to the its growing important in high speed design. Termination is also becoming an important to maintain the constant impedance seen by the signal as it travels down the transmission line and to prevent undesirable reflections.
Let the magnitude of the transmission line propagation function to be $H_x$. When a step voltage of magnitude $V_o$ is applied, the initial value of the signal at the input of the transmission line, using voltage divider rule is:

$$V_{INITIAL} = V_o \frac{Z_o}{R_s + Z_o} \quad (5.1)$$

As the signal propagates down the transmission lines, it is attenuated and distorted (phase shift) by the line propagation function, $H_x$ which is defined as

$$H_x = e^{-X[(R + j\omega L)(G + j\omega C)]^{1/2}} \quad (5.2)$$

Voltage reflection coefficient at load side describes the fraction of the voltage signal that is reflected back to the source and is defined as:

$$\rho_L = \frac{R_L - Z_o}{R_L + Z_o} \quad (5.3)$$

Voltage transmission coefficient describes the fraction of the incident signal voltage that is transmitted through the interface into the load and is defined as:

$$\tau_L = (1 + \rho_L) = \frac{2R_L}{R_L + Z_o} \quad (5.4)$$
The reflected signal is again attenuated by $H_X$ as it travels back to the source and the source end reflection coefficient describes fraction of the voltage signal reflected back to the load end again as follows:

$$\rho_s = \frac{R_s - Z_o}{R_s + Z_o} \quad (5.5)$$

The strength of the first signal emerging from the load side is obtained as follows:

$$V_{TX0} = V_{initial} H_X (1 + \rho_L) \quad (5.6)$$

The second signal reflected off the source to emerge back at the load is given by:

$$V_{TX1} = V_{initial} H_X [H_X^2 \rho_L \rho_s] (1 + \rho_L) \quad (5.7)$$

Subsequently, the emerging signals are characterize by:

$$V_{TXN} = V_{initial} H_X [H_X^2 \rho_L \rho_s]^N (1 + \rho_L) \quad (5.8)$$

The equation at the load after $N$ reflections is obtained by summation of all the emerging signals and the closed form* equivalent for this infinite geometric series is:

$$V_w = \frac{V_{initial} H_X (1 + \rho_L)}{1 - H_X^2 \rho_L \rho_s} \quad (5.9)$$

5.1.3 Lattice Bounce Diagram

To illustrate that without proper terminations, the effects of transient reflections as a result of mismatch will cause signal distortion in the form or ringing as describe in 5.1.2 will occurs, the transmission line lattice bounce diagram is use here. In a typical real world example, a source impedance of 10 Ω and high impedance at the load side as most typical input of CMOS circuit are high in impedance. Together we design the PCB stack-up and trace width such that we have a characteristic impedance of 50 Ω.

\[
\rho_L = \frac{R_L - Z_o}{R_L + Z_o} = \frac{\infty - 50}{\infty + 50} \approx 1
\]  
\[
\rho_S = \frac{R_S - Z_o}{R_S + Z_o} = \frac{10 - 50}{10 + 50} = -0.667
\]  
\[
V_{initial} = V_0 \frac{Z_o}{R_S + Z_o} = (1V) \frac{50}{10 + 50} = 0.833V
\]  

![Lattice diagram illustrating the effects of signal multiple reflections](image)

Figure 63: Lattice diagram illustrating the effects of signal multiple reflections
Using a 2ns rise time as in typical older slow speed digital design, 1V input step source at 10 MHz, over a 50Ω transmission line with 0.5ns delay. Simulated results in Fig. 64 illustrates the ringing (< 10%) is not a concern even if mismatch occurs. No termination is required.

Figure 64 : Simulated signal at the receiver at the far end of the transmission load side using 2ns rise-time without termination

However, in today’s high speed operations, the rise time in order of pico-second. When using a 0.1ns rise-time, the ringing effects as describe in 5.1.3 earlier becomes obvious and severe (>60%), which is unavoidable if no terminations are used.

Figure 65 : Simulated signal at the receiver at the far end of the transmission load side using 0.1ns rise-time without termination.
With the same 0.1ns rise-time, 0.5ns delay, 50ohm characteristic impedance and source impedance of 10ohms, when the appropriate source series termination (40Ω elected in this simulation) is used, the simulation in Fig. 66 shows that the ringing effects can be control and reduce significantly thus improve the signal integrity. Hence showing the importance of termination in high speed design to avoid signal distortion.

![Simulated signal at the receiver at the far end of the transmission load side using 0.1ns rise-time with source matched termination.](image)

5.1.4 Impedance Matching Technique

To control the reflections, termination can be performed either at the load side known as end termination or at the source side known as source termination.

a) Matching at the Receiver

If the impedance of the receiver is match to the transmission line characteristic impedance, then the reflection coefficient at the load is zero. Effectively, this eliminates the first reflection the moment the signal travels down the transmission line and hit the load termination and this requires the following condition.
The above is true when the load is match to the transmission line. Matching at the receiver can be easily done. For example, simply by putting a shunt resistor ($R_{\text{ShuntR}}$) with value equal to the characteristic impedance ($Z_o$) as shown below.

$$R_{\text{receiver}} = Z_o \implies \rho_L = 0$$  \hspace{1cm} (5.13)

Since the typical input impedance of most CMOS IC input are high impedance, much higher than the matching shunt resistance, the combine parallel impedance at the load will be equal to the shunt resistor which is equal to the characteristic impedance.

$$R_L \gg R_{\text{ShuntR}} ; \quad Z_{\text{RCV}} = \frac{R_{\text{ShuntR}}R_L}{R_{\text{ShuntR}} + R_L} \approx R_{\text{ShuntR}} = Z_o$$  \hspace{1cm} (5.14)

Hence the effective load reflection coefficient becomes:

$$\rho_L = \frac{Z_{\text{RCV}} - Z_o}{Z_{\text{RCV}} + Z_o} = \frac{Z_o - Z_o}{Z_o + Z_o} = 0$$  \hspace{1cm} (5.15)

To estimate the signal rise time for a typical capacitive load, assuming no reflections occurs due to load termination, the signal response due to the transmitted signal from Eqn. 5.4 is

$$V_o(\omega) = 1 + \rho_L(\omega) = \frac{2Z_L(\omega)}{Z_L(\omega) + Z_o(\omega)} = \frac{2}{1 + \frac{Z_o(\omega)}{Z_L(\omega)}}$$  \hspace{1cm} (5.16)
Since receiver load impedance $Z_L$ is composed of the parallel impedance of the terminator resistor $R_{ShuntR}$ and the input capacitance of the receiver with a value of $C$,

$$Z_L(\omega) = \frac{Z_o}{\omega C}, \quad \Rightarrow \quad \frac{1}{Z_L} = \frac{1}{Z_o} + j\omega C$$  \hspace{1cm} (5.17)

Substituting equation 5.17 into equation 5.16

$$V_S(\omega) = \frac{2}{1 + Z_o} \left[ \frac{1}{Z_o} + j\omega C \right]$$

$$= \frac{1}{1 + j\omega \left( \frac{Z_o}{2} \right) C}$$  \hspace{1cm} (5.18)

Hence, for a capacitive loaded end termination, the above shows that of a simple RC filter response with a time constant of $(Z_o/2)C$.

**Problems with load terminations:**

For end terminations, the driving signal propagates at full intensity directly all the way down the transmission line and all reflections are damped by the terminating resistor. Most TTL and CMOS logic gates may not have sufficient current to drive these end terminators.

At steady state, the impedance seen by the source reduces from $R_L$ to $R_{ShuntR} = Z_o$ (since $R_L > R_{ShuntR}$). This increases loading resulting in greater current and $I^2R$ losses leading to higher power consumption for such termination scheme which is critical consideration in today low power and battery operated environment. Assuming the transmission line is not so long that it disperses the signal, so we can let $H_x$ to be unity. Hence, at steady state receiver voltage magnitude also reduces as follows:

$$V_{RCV} = \frac{V_{initial} H_x (1 + \rho_L)}{1 - H_x^2 \rho_{l,s}} = V_{initial} H_x = V_0 \frac{Z_o}{R_s + Z_o}$$  \hspace{1cm} (5.19)
b) Matching at the Source

If the impedance of the source is match to the transmission line characteristic impedance, then the reflection coefficient at the source is zero. Hence this effectively eliminates the reflected signal back towards the source which is damped at the source termination. This requires the following condition:

\[ Z_{\text{Source}} = Z_o ; \ \rho_s = 0 \]  \hspace{1cm} (5.20)

One of the most common methods of source matching is to insert a series matching resistor \( R_{\text{Series}} \) at the output of the driver as follows:

The series matching terminator \( R_{\text{Series}} \) is set such that the combine impedance looking into the source, the series terminator (\( R_{\text{series}} \)) together with the source internal series resistance (\( R_s \)), to be equal to the transmission line characteristic impedance \( Z_o \).

\[ Z_{\text{Source}} = R_{\text{Series}} + R_s = Z_o \]  \hspace{1cm} (5.21)

Hence, the effective source reflection coefficient (\( \rho_s \)) will becomes zero as follows:

\[ \rho_s = \frac{Z_{\text{Source}} - Z_o}{Z_{\text{Source}} + Z_o} = \frac{Z_o - Z_o}{Z_o + Z_o} = 0 \]  \hspace{1cm} (5.22)
When driving a receiver which is typically a high impedance and capacitive in nature with a value of C. Looking back to the source, we see a drive impedance equal to $Z_o$. We would get a response that looks like a simple RC low-pass filter with a RC time constant

$$\tau = Z_o C$$

For a 10-90%, the rise time of the RC filter

$$T_{10-90} = 2.2 R_{eq} C_{eq}$$

$$T_{10-90} = 2.2 Z_o C \quad (5.23)$$

Hence, when capacitively loaded in most digital circuit receiver, the rise time is twice as long as the end-terminated circuit whose $R_{eq} = Z_o / R_{shunt} = Z_o / 2$. With slower rise time, usually smaller residual reflections that the end termination.

The driving waveform is cut half by the series termination before propagating into the transmission line at half intensity. At the receiver far end, a typical CMOS circuit ($R_L$ is large or behave like an open circuit), the signal load reflection coefficient would be ~1. Hence the incoming half voltage together with the half voltage reflected at the receiver will bring the instantaneous voltage to a full level.

At steady state, the impedance seen by the source is $Z_L$ which is typically high impedance for most CMOS circuit. The current requires is therefore much lower and hence lower power dissipation. The steady state voltage across the receiver would be almost equal to the full input driving signal without any reductions.

$$V_{RCV} = V_o \quad (5.24)$$

**Reason for Series Terminations Selection**

Source terminator as shown have a slower rise time, smaller residual reflections, lower power consumption and full receiver voltage compared to the end terminator, hence the reason for its popular applications.
It is often easier to eliminate reflections at the source which is typically resistive (with a little inductance), while mismatch cause by capacitive load when attempting end termination are often worse and complex. Typically source termination, if terminated correctly, will yield near zero reflection coefficient as compared to the end terminator, leading to flatter overall frequency response.

5.1.5 Challenges in Source Matching

Source impedance matching requires the driver internal resistance $R_s$ together with the series terminator must match the transmission line characteristic impedance.

$$R_{Source} + R_s = Z_o$$ (5.25)

The question is how can we determine the device internal resistance ($R_s$) accurately?

Typical driver are has low output impedance but exact is unknown. Even TTL and CMOS circuit output impedance have slight different values in their High and Low states. Hence is always never easy to determine the correct source series terminator.

If we have a good model for the driver either SPICE, a good estimate of the output impedance can be extracted using simulations. However many times, the SPICE model is almost not available as critical design proprietary details of the buffers and latest information can be obtained. Instead a general SPICE model is often given instead which may not necessary be the best representation of the device.

As for IBIS, as describe in section 2.2.2, these are typical models suitable for general simulation and not suitable for high speed application. Often designer has to validate and modify the model for in-house usage but this is often costly and manpower intensive [75]. Still IBIS models for many devices are not readily available [70-72] and lack of accuracy for SI simulation [73-74] which has been the key problems with users.

---

5.2 Measurement of Output Impedance of Clock Driver

As mentioned in Chapter 1, the importance of interconnects termination designs in high-speed digital design is crucial for SI performance. With integrated circuits (ICs) operating at much faster edge rates, proper terminations to ensure good impedance matching become indispensable for functional reliability in high-speed digital systems. Excessive and prolong overshoot can damage devices, and together with undershoot, they cause eye closure in the eye diagram, which can lead to intermittent false triggering. Much work in the area of interconnect terminations has been well reported in the 90s [99-102]. There were earlier works on mathematical models on transmission lines with resistive termination as early as the 60s [103,104].

When circuit designers deal with impedance matching, the main issue is that the IC electrical characteristic not only varies with manufacturing process but also changes significantly with operating conditions, such as supply voltage, operating frequency and temperature, leading to variation in the IC’s output impedance [105]. Such variation poses challenges to the circuit designer to determine the appropriate value of the termination impedance. Although on-chip termination [106-109] has been used to minimise the reflections, the implementation can be very complex requiring impedance control circuitries, optimised driver output design against process, voltage and temperature variation and not forgetting the difficulty in overcoming the effects of on-die resistor non-linearity. In most cases, typical circuit/board designers do not have the luxury of requesting such special features in the ICs that they used.

Due to its simplicity and ease of implementation, source series termination, where the IO driver output is matched to the PCB trace characteristic impedance to achieve optimised SI, is the most commonly adopted technique for impedance matching. It also has the advantage of no component between DC bus and ground. It is also less sensitive to physical series resistor placement as compared to parallel terminated circuits [110]. In source series termination design, the knowledge of the device output
impedance is crucial in determining the precise value of a series resistor for impedance matching. It is very much dependent on the driver output impedance and the PCB trace’s characteristic impedance. The trace impedance is a result of the PCB stackup design and is well controlled during fabrication and its value can be measured easily by means of a time domain reflectometer (TDR) as shown in Fig. 69.

![TDR impedance measurement using Tektronix DSA8200 with P8018 TDR probe](image)

Figure 69: TDR impedance measurement using Tektronix DSA8200 with P8018 TDR probe

However, the selection of the series terminator often requires trial and error process during the prototyping phase. As for the clock driver’s output impedance, only the nominal or typical value is usually given and its accuracy is not guaranteed. Also the output impedance can vary with different operating conditions. Although IBIS models are available, they are not fully validated and users have to ensure their correctness before using them.

The in-circuit two-probe method provides a relatively simple, reliable and accurate means to determine the output impedance of an active device under its intended operating conditions. Accurate extraction of the device’s output impedance at the actual operating condition allows precise selection of series resistor to match the device’s output to the characteristic impedance of the connecting trace on the PCB.
In this section, a practical case study of an actual clock driver and its output series termination selection will be used for demonstration purposes. The procedure to extract the output impedance of the clock driver will be described. The device output measurement results obtained using the two-probe approach will be used for the selection of correct source series termination. Finally, validation with the simulation results for optimised SI performance will be demonstrated.

5.3 Case Study on Series Termination Selection

In most high-speed clock circuit designs, impedance matching is crucial to ensure good SI performance. The choice of proper trace termination can be tedious and often requires several iterations to finalise the correct value to be used. In this case study, the selection of series termination for a high-speed clock driver circuit and its effect on the far-end receiver output waveform will be shown. Two clock drivers from the same manufacturer, one for the actual circuit and the other an alternative part replacement are chosen for the study. The two clock drivers chosen for the design are:

- Texas Instrument 200 MHz clock buffer (CDCV304PW); and
- Texas Instrument 200 MHz PLL clock driver (CDCVF2505).

These two clock drivers are specifically chosen for two reasons. In terms of physical sizing, both parts have the same package type (8 pins TSSOP) with the same PCB footprint so that each can be a direct drop-in replacement for the other. In terms of electrical specification, both are capable of clocking up to 200 MHz. The output series termination is chosen such that the fastest rise and fall times are achievable without compromising on the overshoot or undershoot, which is set to be less than 20% (0.66V) of output steady state voltage of 3.3V.
5.4 Clock Driver Circuit for Case Study

Single ended clock distribution tree is commonly used in systems running on clock speed of less than 100 MHz. The clock circuit used in this case study is shown in Fig. 70(a), which is a typical point-to-point direct interface with series termination for impedance matching. It is part of a high-speed clock prototype developed to study the various high-speed design rules and techniques, such as stub effects, serpentine delay and termination. The fabricated FR-4 PCB for the clock circuit is shown in Fig. 70(b).

Figure 70: (a) Schematic of the application clock driver circuit (b) PCB layout
With the clock driver CDCV304 in the circuit, a few values of series terminations are tested on the board. The measured receiver waveforms for three different values of series terminations are shown in Fig. 71. The best value of $R_s$ is selected based on the optimal signal integrity response that gives the fastest rise-time while keeping the overshoot within +/- 20% (0.66V). Based on the measured waveforms, though the 18Ω termination has the fastest achieve rise time, but the overshoot exceeds the 0.66V criteria. Instead, the 27 Ω is found to be the best choice for series termination as the receiver waveform exhibits the optimal SI performance. Its rise time is as fast as that of the 18Ω termination while the overshoot is kept within specifications at 0.42V.

![CLK304: Comparison of Waveform at RCV](image)

**Figure 71**: Waveform at the receiver end of the transmission line with CDCV304PW

However, when the clock driver is replaced with the alternative replacement part (CDCVF2505), it is found that termination between 22 – 30 Ω are no longer providing similar SI performance as the rise time are degraded. Instead, the 10 Ω series termination provides the most optimal SI performance as shown in Fig. 72 with the fastest achieved rise-time and yet the overshoot stays within the limits.
Figure 72: Waveform at the receiver end of the transmission line with CDCVF2505PW
5.5 Extraction of Clock Driver Output Impedance

To investigate the difference in the series termination values for the two seemingly similar clock drivers, the two-probe method will be used to extract the output impedance of the clock driver under its in-circuit operating conditions. As the current probes do not require direct electrical contact to the clock driver, the proposed method minimises the loading effect and disturbances to the clock driver circuit. Also, with a pre-measurement characterization process, the method has the ability to eliminate measurement error contributed by the measurement setup as mentioned in Chapter 3. For the measurement result, only the impedance magnitude will be shown. The measurement setup to extract the output impedance of the clock driver is shown in Fig. 73.

![Fig. 73: Measurement setup to extract the output impedance of the clock driver](image)

The setup consists of two identical current probes (Model: Tektronix CT-6, bandwidth 500 kHz to 1.5 GHz) coupled to the output of the clock driver circuit inductively without direct connection. Both probes are connected to a Vector Network Analyzer (Rohde & Schwarz ZVB8 bandwidth 150 kHz-8.5 GHz). Port 1 of a VNA injects an AC signal into the clock driver output circuit through the injecting probe and port 2 of the VNA measures the resulting coupled signal in the same output circuit through the receiving probe. By reflecting the impedances of the current probes to the output circuit loop, the equivalent circuit of the output circuit loop is given in Fig. 74.
CHAPTER 5: MEASUREMENT OF ACTIVE DEVICE IMPEDANCE FOR SI ANALYSIS

Figure 74: Simplified equivalent circuit of the two probe measurement setup

\[ Z_{\text{OUT}} \] is the output impedance of the clock driver to be determined, \( Z_{M1} \) and \( Z_{M2} \) are the reflected impedances of the injecting and receiving probes into the clock driver output circuit loop respectively. \( V_{M1} \) is the induced signal voltage in the loop from the output signal source of port 1 of the VNA. \( R \) is a resistor (47 \( \Omega \)) to emulate the output circuit termination to the device and is chosen according to the actual circuit operating condition. \( L \) and \( r \) are the effective clock driver loop inductance and resistance at the clock driver output circuit respectively.

Based on the same techniques described in Chapter 3, the resultant current flowing in the coupling loop due to the injecting signal is given by:

\[
I = \frac{V_{M1}}{R + Z_{M1} + Z_{M2} + r + j\omega L + Z_{\text{OUT}}} \tag{4.7}
\]

Since only the impedance of the clock driver (\( Z_{\text{OUT}} \)) is of interest, the other impedances in the circuit loop due to the measurement setup are grouped together as \( Z_{\text{setup}} = R + Z_{M1} + Z_{M2} + r + j\omega L \). Then, equation (4.7) can be simplified as follows:
\[ I = \frac{V_{M1}}{Z_{\text{setup}} + Z_{\text{OUT}}} \]  \hspace{1cm} (4.8)

The unknown output impedance of the driver \( Z_{\text{OUT}} \) under in-circuit condition can be determined using the following equation.

\[ Z_{\text{OUT}} = \frac{kV_1}{V_2} - Z_{\text{setup}} \]  \hspace{1cm} (4.9)

By replacing \( Z_{\text{OUT}} \) with a known precision standard resistor \( R_{\text{std}} \) (\( Z_{\text{OUT}} = 50 \, \Omega \)) and then with a short (\( Z_{\text{OUT}} = 0 \, \Omega \)) during the pre-measurement calibration process, the impedance introduced by the measurement setup can be eliminated. Once \( Z_{\text{setup}} \) and \( k \) are found using (3.18) and (3.19), respectively; the measurement setup is ready to measure the unknown output impedance of the clock driver, \( Z_{\text{OUT}} \).
5.6 Clock Driver Output Impedance Measurement Results

For the extraction and validation of the clock driver output impedance, a test circuit is developed and fabricated as shown in Fig. 75. With the test circuit, the output impedances of the CDCV304 and CDCVF2505 clock drivers will be extracted.

Since the two clock drivers have the same PCB footprint, only a PCB test jig is needed. It will be shown later that both devices though look similar, have very different output series termination value for matching purposes. The in-circuit measurement setup for the clock driver under test is shown in Fig. 75.

![Figure 75: Schematic of the clock circuit test prototype](image)

Fig. 76 shows the fabricated FR-4 printed circuit board (PCB) to be mounted with the clock driver to emulate the actual in-circuit operating condition. A jumper (W2) at the input of the clock driver allows it to activate static logic “High” or “Low” logic level. The SMA connector to the input (SMA-P1) allows an external clock signal for continuous logic changes. The clock output pin connects to a resistor pad (R1) for series source termination prior to the 6 inch, 50 Ω microstrip. Provision for a direct load (R2) whose value is very closed to the actual driver output loading is chosen. In our case, a 47 Ω is selected. Two jumper pads (W3 & W4) are catered for insertion of the CT6 probes to measure the clock driver's output impedance. The zoom in view of the measurement setup with the current probes is shown in Fig. 77.
Figure 76: PCB layout of circuit under test for CDCV304PW

Figure 77: Actual two probe measurement test setup with device 1: CDCV304PW.
In general, the procedure mentioned in Chapter 3 is adopted with some slight variation. In order to extract the impedance of the clock driver output before the series termination $R_1$ prior to its connection to the transmission line, the test circuit incorporated an additional connected load resistor $R_2$. The value of $R_2$ is chosen such that it emulates the actual circuit load termination, which in this case is the 50 $\Omega$ oscilloscope at the far end of the transmission line. The load resistor $R_2$ must be placed very close to the series termination $R_1$ so as to characterise the driver as close as possible to the point of interface, as shown in Fig. 78.

![Pre-calibration setup to characterise the clock driver device 1: CDCV304PW.](image)

For the pre-measurement calibration process, $R_1$ is removed and only the clock driver output and $R_2$ is connected. By the same calibration procedure using 0 $\Omega$ (direct short) and 50 $\Omega$ standard resistor in place of the clock driver output, the two unknown, $k$ and $Z_{\text{setup}}$ can be found in this calibration process.

The magnitudes of $Z_{\text{setup}}$ and $k$ versus frequency up to 1 GHz are given in Fig. 79 and Fig. 80, respectively. Fig. 79 shows $Z_{\text{setup}}$ is nearly constant at 47 $\Omega$ (dominated by $R_2$) but at about 600 MHz, the loop inductance of the output loop of the clock driver begins to kicks in. Based on the $Z_{\text{setup}}$ measurement, the inductance is found to be around 20 nH. From Fig. 76, the circuit loop inductance consists of 18 mm of the PCB trace length, two 5 mm conductors for the placements of current probes and the equivalent series inductance of $R_2$. The PCB trace is designed to have a characteristic impedance of 50 $\Omega$ with a trace width of 2 mm, trace thickness of 0.0356 mm and trace height of 1 mm. The 18 mm trace length works out to be 5.36 nH. The inductance of each 5 mm conductor is found to be 2.5 nH and the equivalent
series inductance of the resistor (from the manufacturer data sheet) is 9.12 nH. The total resultant inductance is 19.48 nH, which agrees rather well with the earlier estimated value of 20 nH from the measured Zsetup.

![Figure 79: Magnitude of Zsetup versus frequency](image1)

Figure 79 : Magnitude of $Z_{\text{setup}}$ versus frequency

Similar to the explanation in section 4.3 for Fig. 55, Fig. 80 here shows that $k$ remains constant at 1 $\Omega$ and becomes frequency dependent above 800 MHz due to the effect of parasitic capacitance of the primary coil of the probe.

![Figure 80: Magnitude of k versus frequency](image2)

Figure 80 : Magnitude of $k$ versus frequency
With the values of \( k \) and \( Z_{\text{setup}} \) determined, the setup is ready to measure the output impedance of the clock driver. The circuit is first characterised under static condition with input kept at "3.3V" logic High and then at "0V" logic Low. The input is driven by a 1 MHz clock. The results are shown in Fig. 81(a). Next the circuit operating in a dynamic mode with input now excited by a 10 MHz clock signal, the measured output impedance of the clock driver for CDCV304PW is found to be around 23 \( \Omega \), as shown in Fig. 81(b).

This is in line with the value of the typical impedance of the CDCV304 LVCMOS output [114] of around 20 \( \Omega \). Above 700 MHz, the clock driver output impedance exhibits inductive behaviour. Based on the measured impedance of 50 \( \Omega \) at 1 GHz as shown in Fig. 81, the estimated inductance is about 4.3 nH, which is the typical lead frame and wire bonding inductance to be expected. Hence, to match with the 50 \( \Omega \) microstrip line, the output series termination resistor of around 30 \( \Omega \) is recommended. In our case, since the measured output impedance was found to be 23 \( \Omega \), the series termination of 27 \( \Omega \) will provide best impedance matching to the microstrip line for optimal SI performance.

![Clock Driver Output Impedance Response (CDCV303PW)](image)
Figure 81: Measured clock driver output impedance for CDCV304PW (a) Static high, static low and 1 MHz and (b) Dynamic, 10 MHz

However, the measured output impedance for CDCVF2505 is found to be 45 Ω, as shown in Fig. 82, which is nearly two times larger than that of CDCV304PW. This is due to the additional internal 25 Ω output resistance of the clock driver. Based on the measured impedance of 196 Ω at 1GHz, the estimated inductance is 24 nH which is much higher than the CDCV304PW. This is the additional inductance to be expected due to the added equivalent series inductance of the embedded series resistor. The output impedance stays constant at 45 Ω and increases with frequency above 300 MHz due to the inductive effect of the internal output resistance, which is rather common for small-value resistor.
The datasheet of CDCVF2505 clock driver shows an additional embedded output series resistor of 25 $\Omega$ [115]. Further search on the manufacturer website [116] shows a more detailed output characteristic of the CDCVF2505 clock driver as shown in Fig. 83. The estimated total output impedance is approximately between 37 $\Omega$ and 40 $\Omega$. Based on the actual measured clock driver output impedance of 45 $\Omega$, a series termination of around 5-10 $\Omega$ would provide the best matched condition to the microstrip line.
5.7 Validation with Simulation Results

The clock driver circuit will be simulated using Computer Simulation Technology Microwave Studio (CST-MWS) and Design Studio (CST-DS). The IBIS models of both clock drivers are obtained from manufacturer website while the layout of FR-4 printed circuit boards (PCB) will be imported into CST simulation environment in Gerbel format. The simulated circuit shown in Fig. 84 consists of the clock driver, the source output series terminator (R1) and a 6” 50Ω transmission line. The far-end load termination of the transmission line consists of a 3 pF capacitor in parallel with a 40 kΩ resistor emulating the Tektronix TAP3500 probe loading.

![CST-DS IBIS transient simulation setup](image)

With the IBIS model and Gerbel imported to the CST time-domain simulator, a parameterised sweeps on the output series terminator RS across a range of values from 10 to 30 Ω for CDCV304 and 0 to 20 Ω for CDCVF2505 are performed. The output overshoot behaviour at the receiver end is simulated and shown in Fig. 85.
The simulated results are consistent with the measured results shown previously. Both simulated and measured results indicate clearly that although the clock drivers look similar, but their output impedances can be significantly different. Therefore, when the same series termination resistor is used, the SI performance can be drastically different. For CDCV304, the output resistance is around 25-30 $\Omega$ and hence an output source series termination resistor of value 30 $\Omega$ is a good choice. However, it is not suitable for CDCF2505, which contains an integrated output series resistor of 25 $\Omega$ making the total output impedance to be around 40 $\Omega$ [116]. Hence, the source series termination resistor should be changed to 10 $\Omega$ instead for optimal SI performance.

The practical case study in this section has demonstrated the ability to extract the output impedance characteristic of the clock driver under its intended operating condition, which is very useful on proper series termination design to achieve optimised SI performance.
5.8 Experimental Validation with Measurement Results

The clock driver circuit is designed and fabricated for this experimental measurement validation purpose. With the extracted clock driver output impedance, it allows accurate selection of the series terminating resistor at the output of the clock driver for matching to the transmission line to achieve optimal SI performance. The actual circuit shown in Fig. 75 consists of the clock driver, the source output series terminator (R₁) and a 6” 50Ω transmission line. The board is powered up by a 5V source through a 3.3V regulator. A repetitive square pulse of 25 MHz, 3V amplitude with 50 % duty cycle is connected to the input of the clock driver from Tektronix arbitrary function generator (AFG 3101). The signal waveform at the far end of the microstrip line is measured with a Tektronix digital phosphor oscilloscope (DPO 7354 3.5 GHz).

For the first clock driver, CDCV304PW, its extracted output impedance is 23 Ω and therefore a series resistor of 27 Ω is chosen for optimal SI performance. Fig. 86 shows the signal waveform measured at the far end of the microstrip line with a 27 Ω series resistor. To illustrate the effect of unmatched condition, the measured waveform with a 5 Ω series resistor is included in Fig. 86. As expected, the measured waveforms for both cases show clearly that with the 27 Ω series resistor, the waveform exhibit minimum signal reflections when compared to that with the 5 Ω series resistor.

![Clock Signal at Far-End of Microstrip Line CDCV304PW](image)

**Figure 86:** Measured clock waveform at far-end of microstrip line with CDCV304PW
For the second clock driver CDCVF2505 with extracted output impedance of 45 Ω, a series resistor of 5 Ω will provide the optimal SI performance. Fig. 87 shows the measured waveforms at the other end of the microstrip line for both 5 Ω series resistor and 27 Ω series resistor. The measured waveforms indicate that the 5 Ω series resistor has minimal signal slew as compared that with the 27 Ω resistor. This shows that the 27 Ω series resistor is too large a value to match this CDCVF2505 clock driver to the microstrip line causing the signal waveform to degrade.

![Clock Signal at Far-End of Microstrip Line CDCVF2505](image)

**Figure 87:** Measured clock waveform at far-end of microstrip line with CDCVF2505

The measured results demonstrate that the ability to extract the output impedance of the active clock driver under its actual operating condition allow precise selection of the series resistor value for good SI performance and eliminate the usual trial-and-error design process.
5.9 Impact of Series Termination on Rise-time and Emission

To ensure optimised SI, one also has to take note of the EMI emission control in the circuit design, especially when series termination selection is concerned. Too large a series terminator can suppress the EMI emission but it is at the expense of reduction in signal rise-time and hence SI. Therefore, a balance approach has to be adopted. Using the time-domain circuit simulation on CST Design Studio with CDCV304PV clock driver IBIS and actual PCB Gerbel imported, the circuit shown in Fig. 88 will be simulated. The resulting time-domain signal received at the far-end of the transmission line with different series termination resistors are shown in Fig. 89.

![CST-DS IBIS circuit simulation setup with CDCV304PV clock driver](image)

**Figure 88:** CST-DS IBIS circuit simulation setup with CDCV304PV clock driver

From EMI emission point of view, it is often easy to use a larger series termination resistor to reduce the emission, as shown in Fig. 89(c). However this comes at the expense of significant reduction in the signal rise time as shown in Fig. 89(d). Such slew in signal rise-time is undesirable especially in high-speed applications.
Figure 89: Simulation result (a) $R_s=15 \ \Omega$ (b) $R_s=24 \ \Omega$ (c) $R_s=50 \ \Omega$ (d) receive signal
Chapter 6

6.0 CONCLUSION

With increasing importance of SI in today’s high-speed digital circuit design environment, the major challenge is to ensure that the circuit is not only functionally working but also electrically compliance to tighter specifications and design margin.

Source series termination to match the driver output impedance to the PCB trace characteristic impedance to ensure optimal SI performance is one of the most commonly adopted matching techniques used today for its simplicity and effectiveness. To ensure good impedance matching, the output impedance of the driver has to be known before a proper series termination is chosen to match to the PCB interconnection trace with confidence.

6.1 Major Contribution of the Thesis

The major contribution of this thesis is the successful extension of the inductive non-contact two-probe measurement technique to 1GHz. To ensure the accuracy up to 1 GHz, a pre-measurement error elimination process has been developed so that one could accurately characterizing the impedance of a device’s output impedance under its intended operating conditions.

The proposed two current probes measurement technique has been described and validated in the characterization of passive components under in-circuit operation with varying biasing conditions. [117] The measured results provide an insight of the impedance behavior of a critical component under its intended biasing condition so that the proper choice of the component can be made in circuit design to achieve
appropriate and optimal performance. Especially for passive component with non-linear behavior, the proposed in-circuit measurement technique has the ability to detect the change in impedance due to varying biasing conditions.

The technique is then extended to determine the output impedance of an in-circuit active device under its intended operating conditions. [118] It is found to be very useful for selecting proper series termination for high-speed clock drivers. With the known extracted output impedance of the driver, a source series termination can be easily chosen to optimize the SI performance as well as to minimize EMI emission. With the proposed technique, it eliminates unnecessary trial-and-error for manual tuning the series termination value.

The proposed in-circuit measurement method can be further extended in many potential applications. For example, it allows the characterization of unknown power supply output impedance and a noisy digital module input impedance for designing an EMI filter systematically [119,120].
6.2 Limitations and Recommended Future Research Work

The proposed approach is not without limitations. The major limitation of this approach is the operating bandwidth of the current probe itself. The upper frequency limit of the current probe determines the maximum frequency of the proposed measurement approach. Hence, better designed high frequency current probe is necessary in order to extend the operating bandwidth further.

In the active device output characterisation, the proposed technique also has its shortfall. Firstly, it is intended for device level characterisation on a standalone dedicated test jig. As illustrated in the active device output characterisation setup, in order to perform the in-circuit characterisation, several provisions in the PCB layout has to be taken into consideration at the design stage for the placement of current probes and bypass resistor. However, this can be kept to a minimum area using surface mount pads. Still this occupies an area in the PCB board, which the designer has to cater for if in-circuit characterisation is truly needed.

Based on the author opinion and his research in this area, the following future works are worth exploring:

a) Modification improvement can be made to the test jigs design to cater for proper device adapters such as chip holders for passive component and IC sockets for active devices. This allows ease of device testing without the need for soldering and de-soldering, hence minimising damage to the DUT. Note that during pre-calibration, the effects of the socket are being taken into consideration and will be eliminated.

b) Currently the results obtained from the VNA are imported into Microsoft Excel spread sheet to generate the graph. It would be useful and practical if programming effort is made to develop the routine to be integrated into full device test software so as to automate this process and the report generation during the characterization procedure.
c) The two probe measurement approach can be used in the in-circuit characterisation of EMI filter to investigate the impact of loading on the filter attenuation, an area that can be useful for the designer.

d) Another area that is worth exploring is the use of the proposed method to extract the input power supply impedance of an integrated circuit (IC) for the purpose of characterisation of its power distribution network (PDN) impedance for optimal decoupling design. Some preliminary work by the author on the power supply impedance has been reported in [119,120].
Author’s Publications

Journal Papers


Conference Papers


Bibliography


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### Appendix A: List of EDA Vendors and Tools

<table>
<thead>
<tr>
<th>Company</th>
<th>Product</th>
<th>Website</th>
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Company: **ComSol Group (1997)**  
Product: ComSol Multiphysic 3.3 2006  
Include AC/DC, Acoustics, CAD import, Heat transfer, RF, MEMS and Structure Mechanics  
Website: [http://www.comsol.com](http://www.comsol.com)

Product: Scalable Verification, IC Nanometer Design, PCB-FPGA system design  
System Level Design, Embedded systems (EDGE, Nuclues), DFT,  
Modeling, Electrical System design and harness engineering  
IP (USB, Ethernet, PCI Express, Serial ATA, Peripheral, Mixed signal)  
Modelsim Digital simulation, ADVance MS/RF mixed signal simulator  
Hyperlynx Ext/GHz - Board level SI, crosstalk and EMC analysis suite  
ICX - advance electrical driven design and board/system level verification  
DxSim & DxDesigner - Board simulation and verification environment  
QuietExpert - Rule based PCB SI, EMC and layout verification system  
Website: [http://www.mentor.com](http://www.mentor.com)

Product: Cadence Encounter - Digital IC (nm Soc) design platform  
Cadence Virtuoso - Custom IC silicon design platform  
Cadence Allegro System - IC-PKG-PCB Interconnect co-design platform  
Cadence SiP - System level Digital/RF SiP co-design with advance packing  
Cadence Incisive - Functional verification platform for large complex chips  
Cadence Orcad, DFT and Cadence Kits & IP  
Website: [http://www.cadence.com](http://www.cadence.com)

Product: MWO 2007 Microwave Office - Microwave/RF design platform  
ACE Automated Circuit Extractor  
VSS 2007 Visual System Simulator - Complete, end-end comms system design  
Analog Office Open RFIC design platform  
AWR SI 2006 Cross Domain Signal Integrity Co-chip/pkg/module Solution  
AXIEM 3D planar EM simulator (soft launch Sep2007)  
Website: [http://web.appwave.com](http://web.appwave.com)